34. (Amended) An emitter, comprising:

an electron supply surface;

an insulator layer formed on the electron supply surface and having a first opening defined within;

an adhesion layer disposed on the insulator layer, the adhesion layer defining a second opening aligned with the first opening;

a conductive layer disposed on adhesion layer and defining a third opening aligned with the first and second openings;

a tunneling layer formed on the electron supply layer within the first, second, and third openings; and

a cathode layer disposed on the tunneling layer and portions of the conductive layer, wherein the portion of the cathode layer on the tunneling layer is an electron-emitting surface wherein the emitter has been subjected to an annealing process.

REMARKS

The Title of the Invention, the Specification, and the Abstract have been amended. Claims 1, 7, and 34 have been amended. Claims 1-71 remain in the application, although claims 18-20 and 41-71 have been withdrawn from consideration. A marked up version of the claims is found in Appendix A. Further examination and reconsideration of the application, as amended, is hereby requested.

In Appendix B of this Amendment are copies of exhibits used as evidence to support the assertions made herein. The exhibits are supported by a declaration under Rule 132 as required by MPEP 716.02.

Exhibit A is a copy a report dated 1/12/2001 disclosing results of the characterization of non-annealed and annealed versions of the emitter.

Exhibit B is a copy of an status report title "MIS Update – Planfest IV" dated 3/20/2001 which describes emitter test results and failure analysis of emitters using the invention.

Exhibit C is a copy of further tests after the application was filed which demonstrate the nanohole creation formed by the annealing process disclosed in the application.

Exhibit D is a slide showing the emitter test system used to perform the emission testing.

In Section 3 of the Office Action, the Examiner objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because reference sign 36 was not mentioned in the specification. Applicants have amended the specification to include the reference designator 36 thereby making the specification consonant with the drawings. Removal of this objection is respectfully requested.

In Section 4 of the Office Action, the Examiner objected to the Title as being non-descriptive. Applicants have amended the Title to make it more descriptive of at least one aspect of Applicant's invention.

In Section 5 of the Office Action, the Examiner objected to the abstract of the disclosure due to a grammatical error. Applicants have amended the abstract to correct this error. Removal of this objection is respectfully requested.

In Section 6 of the Office Action, the Examiner objected to claim 1 due to an informality. Applicants have amended claim 1 to correct the informality. Removal of the objection is respectfully requested.

In Section 7 of the Office Action, the Examiner notes that independent claims 13 and 14 appear to depend from claim 1, that independent claims 28-30 depend from claim 21 and that independent claim 31 appears to depend from claim 30. Applicants are unsure of the Examiner's purpose for this statement but note that this dependent form of claiming is permissible as held by the Board of Patent Appeals and Interferences in in re Moelands, 3 USPQ.2D 1474 (1987).

It appears that the Examiner may be using this statement in Section 7 of the Office Action for the purposes of preventing the limitations of a respective parent claim from being considered in the examined dependent claims. If so, Applicants respectfully disagree with this interpretation of MPEP 608.01 (n).

Applicants assert that rather then being *independent* claims, claims 13, 14 and 28-31 are proper *dependent* claims that comply with 35 USC 112, 4th paragraph. Each constitute "a further limitation of the subject matter claimed," are not broader than their parent claims. In addition, no element of any respective parent claim is deleted or replaced by any other element in claims 13, 14, and 28-31. These claims incorporate by reference all the limitations of the claim to which each refers as required by 35 USC 112, 4th paragraph. Furthermore, a product which would infringe an integrated circuit of claim 13, the electronic devices of claims 14 and 30, the display device of claim 28, the storage device of claim 29, or the computer system of claim 31 would also infringe the respective parent claim. The Board in in re Moelands noted that they read MPEP §608.01(n) (Dec. 1985) as being consistent with their decision. Accordingly, the Applicants believe the Examiner has made an error in not considering the limitations of the respective parent claim in the examination of claims 13, 28, 14, 16, 17, 29 and 30-33 and requests reexamination and reconsideration of these claims in addition to the additional representations of patentability discussed below.

In particular for claims 13 and 28, the Examiner is Section 9 of the Office Action rejected claims 13 and 28 under 35 USC 102(b) as being anticipated by Nakatani et al. As noted in MPEP 2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." As noted above, claim 13 includes the limitation "the emitter of claim 1 disposed on the substrate" and therefore incorporates the limitations of claim 1 which includes the limitation of "a tunneling layer disposed between the electron supply layer and the cathode layer." Nakatani is directed to a flat display the uses field emission tip emitters that are "conical metal elements each having a sharp tip formed of a metal" (See col. 5, 59-64). Nowhere in Nakatani can the Applicants find "a tunneling layer disposed between the electron supply layer and the cathode layer" that Applicants are claiming. Indeed, the operation of a field emission tip emitter does not require the presence of a "tunneling layer" as it uses high electric field strength only and not electron tunneling under high electric fields for emission. Accordingly, Nakatani does not disclose, teach, or suggest Applicants' claimed invention.

In addition, the Examiner asserts that Nakatani discloses "circuitry for operating the emitter formed on the substrate with the emitter." Applicants respectfully traverse this statement of the Examiner. As noted in the disclosure of Nakatami, "the emitter electrode lines serve as a power supply line to apply a negative voltage (e.g. –40V)" and the "gate electrode lines serve to supply a voltage (e.g. 40V for extracting electrons from the emitter tips" (see col. 5, lines 66-67 and col. 6, lines 11-12). Rather than providing for "circuitry for operating the emitter formed on the substrate with the emitter" as Applicants are claiming, Nakatami merely provides for power and control lines for accessing the emitters as is traditionally done with conventional displays. Indeed, the –40V and 40V differential voltage (80V total) applied to the emitter rules out using conventional control circuitry from being "formed on the substrate with the emitter" as Applicants are claiming. As noted in Applicants' disclosure on page 4, lines 28-30, the emitter of Applicants' claimed invention only requires about 3-10V to operate which is within the range of conventional control circuitry in integrated circuits. One aspect of Applicants' invention provides that the operating voltage that enables the emitter to emit is lowered substantially from prior art voltage levels thus allowing for the "circuitry for operating the emitter" to be "formed on the substrate with the emitter." Accordingly, Nakatani alone or in combination cannot anticipate or suggest Applicants' claimed invention.

In particular for claim 28, the Examiner stated that Nakatani discloses "an integrated circuit including the emitter (3a) wherein the emitter emits a visible light source." Applicants respectfully traverse the Examiner's assertion for several reasons:

First, as noted above, claim 28 depends on claim 21 and thus incorporates the limitations of claim 21. Claim 21 includes the limitation of where the emitter includes "a tunneling layer formed on the electron supply layer in the opening." As noted for claim 13, Nakatani does not disclose, teach or suggest a tunneling layer as Nakatani only discloses using a field emission tip emitter which is a different type of emitter than Applicants' tunneling emitter.

Second, Nakatani does not disclose the limitation of "wherein the *emitter emits* a visible light source" as Applicants are claiming. Indeed, as shown in Fig. 2 of Nakatami, the emitter tips 1 only emit electrons that impinge fluorescent layer 8, which then creates photons that are directed back past the emitter tips 1 to a

watching eye (see col. 9, lines 29-41). Accordingly, Nakatami does not disclose, teach, or suggest that "the *emitter emits* a visible light source" but rather that the emitter emits electrons which "impinge upon the fluorescent layers 8 from which excitation light is emitted."

Third and finally, the Examiner asserts that Nakatani discloses "a lens (8) for focusing the visible light source, wherein the lens is coated with a transparent conducting surface to capture electrons emitted from the emitter. As noted previously, reference 8 is directed to a fluorescent layer and not a "lens for focusing" as Applicants are claiming. Nor does the fluorescent layer 8 include a "transparent conducting surface to capture electrons." Indeed, the fluorescent layer 8 would not be operational if it included a transparent conducting surface that captured the electrons before they were to impinge on the fluorescent layer as it is the electrons striking the fluorescent layer that causes the fluorescent layer to electroluminesc and from which excitation light is emitted.

Accordingly, Nakatani does not alone or in combination with the prior art made of record disclose, teach or suggest Applicants' claimed invention for claims 13 and 28 and removal of the rejection under 35 USC 102(b) is respectfully requested.

In Section 10 of the Office Action, the Examiner rejected claims 14, 16, 17, and 30-33 under 35 USC 102(b) as being anticipated by Xia. As noted previously, claims 14, 16, and 17 depend directly or indirectly on independent claim 1 and thus incorporate the limitations of claim 1. Similarly, claims 30-33 depend directly or indirectly on independent claim 21 and thus include all the limitations of claim 21. Xia is directed to a "Single Pixel Tester for Field Emission Displays" (See title, abstract and col. 3, lines 55-67.) Xia does not disclose, teach, or suggest the limitation of a "tunneling layer" nor that "the emitter has been subjected to an annealing process" as Applicants are claiming in claims 1 and 21 and which is included by way of dependent limitation in claims 14, 16, 17 and 30-33. Accordingly, because "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," Xia does not anticipate claims 14, 16, 17, and 30-33. In addition, as will be discussed below, Applicants believe independent claims 1 and 21 to be patentable over the art made of record. Accordingly, dependent claims 14, 16, 17

and 30-33 are believed patentable based on the patentability of their respective independent claims.

Claim 30 includes the additional limitation of a "focusing device for converging the emissions from the emitter." This limitation is not disclosed, taught or suggested by Xia. At most, Xia discloses an extraction gate or grid structure 15 (Fig. 1 and col. 1, lines 36-37). This extraction grid collects stray electrons but is not used as "a focusing device for converging the emission from the emitter" as Applicants are claiming. Claims 31-33 depend directly or indirectly on claim 30 and are deemed patentable based at least on the patentability of parent claim 30.

Accordingly, for the foregoing reasons, Xia does not anticipate claims 14, 16, 17 and 30-33 and removal of the rejection under 35 USC 102(b) is respectfully requested.

In Section 11 of the Office Action, the Examiner rejected claim 29 under 35 USC 102(b) as being anticipated by Gibson et al. It should be noted for the record that Gibson is commonly assigned to the same assignee as the instant application, i.e. Hewlett-Packard Co. Dependent claim 29 depends directly on independent claim 21 and as earlier discussed includes all the limitations of its parent claim. Accordingly, the storage device of claim 29 includes an "integrated circuit" that includes the emitter of claim 21 which has the limitations of a "tunneling layer" and "wherein the emitter has been subjected to an annealing process." These limitations are not disclosed, taught or suggested by Gibson as Gibson discloses "*field* emitters ... the type that can produce electron beams that are *narrow enough* to achieve the bit density of the storage medium, and *can provide the power density* of the beam current needed for reading and writing to the medium" (see col. 3, lines 39-44). Therefore, Gibson discloses the use of "field emitters" and not an emitter with a "tunneling layer" "subjected to an annealing process" as Applicants are claiming. Nor would it be obvious to substitute a tunneling emitter (also known as a flat (vs. tip) emitter) for the field emitter. In Gibson's application, the emitter must be capable of producing a narrow beam at a sufficient power density to read and write the medium. Conventional tunneling emitters are unable to meet this requirement while Applicants' disclosed and claimed emitters provide a power density 10-1000x (as discussed below) more than that found with prior art tunneling emitters. Thus,

Applicants' annealed tunneling emitters are now comparable in power density of field emitters and allows for operation of the emitter in less stringent vacuum environments thus allowing for higher reliability, lower costs, and less complex packaging. Accordingly, Gibson does not anticipate nor suggest Applicants' claimed invention. Removal of the rejection under 35 USC 102(b) for claim 29 is respectfully requested.

In Section 13 of the Office Action, the Examiner rejected claim 1 under 35 USC 103(a) as being unpatentable over Simmons et al. The Examiner stated that Simmons discloses all the limitations of claim 1 except that of "the electron supply, cathode layer, and tunneling layer have been subjected to an annealing process." The Examiner then states that this limitation makes claim 1 a product by process claim. The Examiner then notes that the Applicant has the burden of proof in such cases as the case law makes clear.

In in re Spada, 911 F.2d 705, 709, 15 USPQ.2D 1655 (Fed. Cir. 1990), the Federal Circuit concluded that the Board of Patent Appeals (PTO) was correct in requiring that an Applicant in a product-by-process claim, upon sound basis that the prima facie case has been made, to have the burden of proof *to show they are not the same structure*. The PTO suggested, and the Federal Circuit agreed, that an Applicant should provide some scientific explanation for the asserted differences between the properties of his compositions and those described by the prior art. The court went on to say that "[w]hile an inventor is not required to understand how or why an invention works, we think that the PTO was correct, in view of the apparent identity of the compositions, in requiring Spada to distinguish his compositions from those of [the prior art]." The court implied that the evidence must relate to the fundamental question of novelty of the claimed invention over the prior art otherwise evidence of unobviousness is superfluous. Id. In Spada, the court stated that the Applicant is *reasonably* required to show that his claimed composition is different from those describe by the prior art.

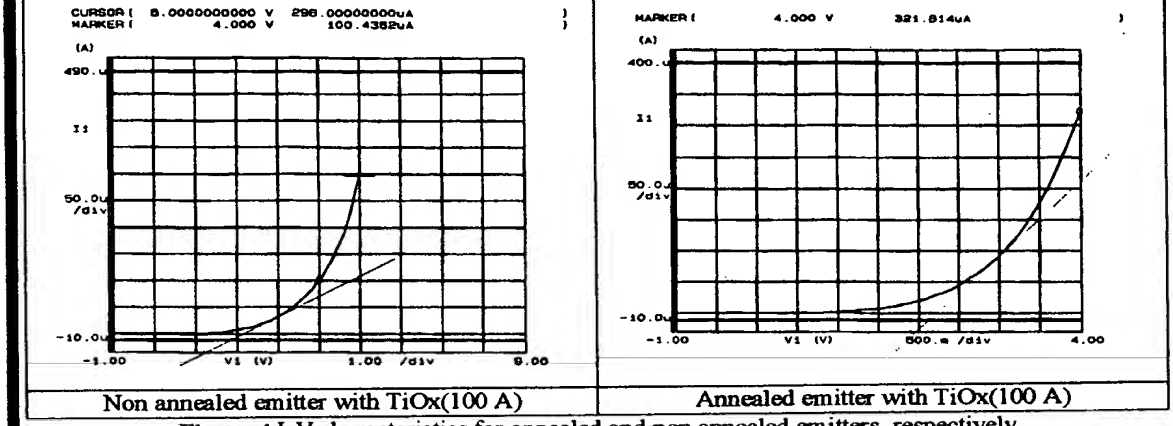
While it is well established that an Applicant for patent need not understand the theory of operation of his invention (Eames v. Andrews, 122 U.S. 40 (1887)), it appears that the Applicants are required to do so to overcome the shift in the burden of persuasion. Accordingly, Applicants have further investigated the remarkable results of their invention and now can further describe the physical

changes and possible theory of operation as to why their process produces a emitter that is physically different in both the kind of structure and the degree of results obtained. Applicants believe that they have clearly shown in the disclosure how to achieve the claimed results even though at the time of filing they did not understand of the difference in structure and theory of operation for the unexpected properties. However, Applicants did detail the unexpected properties. For instance, on page 10, lines 25-32, the Applicants state that the emitter is subjected to an annealing process to increase the amount of electron emission from the emitter and the ability to create photonic emissions. Figs. 12A and 12B are shown and described as two exemplary annealing processes. Other effects of the annealing process include increased device yields and increased operating lifetime. Noticeable physical differences include decreased resistance of the contacts of dissimilar metals which increases the current flow to the emitters.

Since filing of the application, the inventors have performed additional tests to better understand the theory of operation and the physical differences from that of the prior art. Among the differences are that:

1) The metal cluster material (the tunneling layer) series resistance decreases. This is significant because if the tunneling resistance decreases the emitter current will increase for a given emitter efficiency which is the ratio of the emission current over the diode current. This effect allows for higher emission currents for a given applied voltage, or lower applied voltages for a desired emission current. Exhibit A includes a graph of the pre-anneal voltage current graph and a graph of the post-anneal voltage current graph of the tunneling layer. These graphs and a portion the explanation thereof from Exhibit A is reproduced below for reference. The current shown is that current which passes through the diode and is not the emission current. The voltage shown is that voltage applied to the diode to enable the diode current to flow. Please note that at the 4V of applied diode voltage, the diode current increases from 100.4 uA for a non-annealed emitter to 321.8 uA for an annealed emitter, which corresponds to a reduction in tunneling resistance of three times.

Some analyses were done to understand the effect of annealing. Figure 4 showed the I – V characteristics for annealed and non annealed emitter, respectively. It showed that at a fixed voltage, the tunneling current for the annealed emitter is about 3 time higher than non annealed emitter. If we took the slope of voltage versus current, we found that the device series resistance for annealed emitter is 3 times lower than non annealed emitter. Therefore, it suggests that the effective electric field to enhance tunneling is higher for annealed emitter than for non annealed emitter at given voltage.



Non annealed emitter with TiOx(100 A) | Annealed emitter with TiOx(100 A)

Figure 4 I-V characteristics for annealed and non annealed emitters, respectively

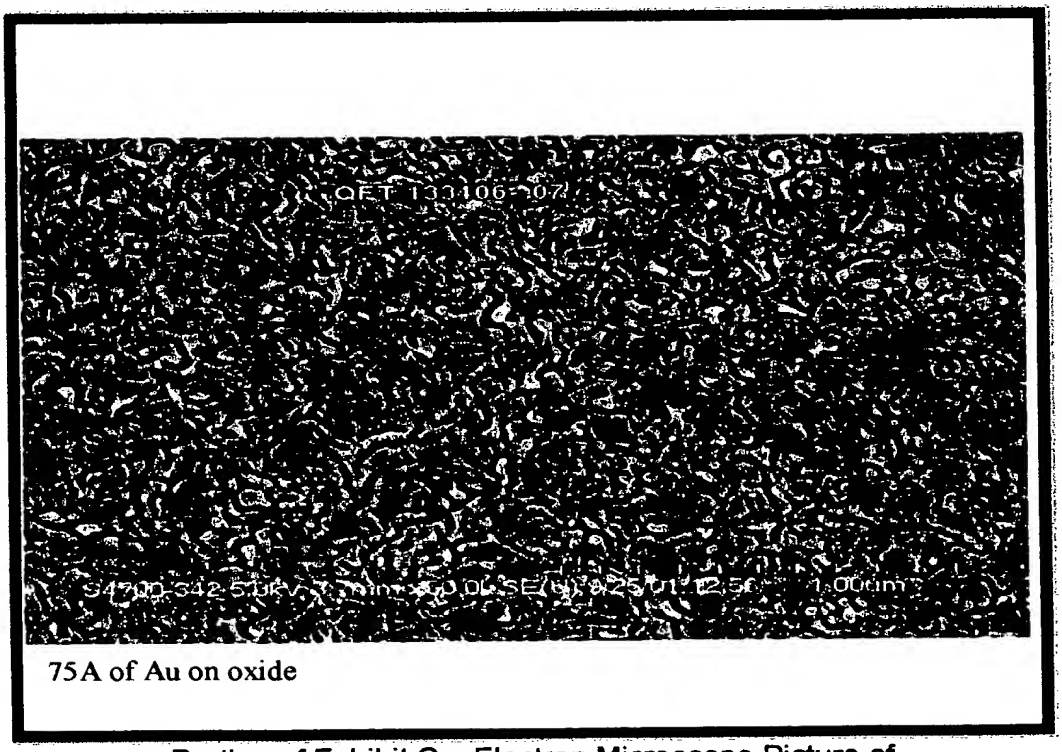
Portion of Exhibit A – Pre and Post Annealing Tunneling Resistance

2) The contact resistance decreases at the interface between the tunneling layer and the electron source, and at the interface between the tunneling layer and the cathode layer. This effect is typical of metal interfaces that are subjected to annealing and would likely be expected.

3) The IV curve for the tunneling emitter changes with time when no annealing step is performed while the IV curve for the tunneling emitter remains constant for an emitter that has been annealed. This is believed to be due to the stress built up in the parts during sputtering. It is believed that during annealing this stress caused by the sputtering is relived and thus allows the part to remain stable. Thus, the annealed emitter has a more consistent emission rate over time than an emitter that has not been annealed or subjected to electroforming.

4) *Most importantly*, the top structure of the cathode layer is transformed during the annealing process to create *nano-sized pinholes* or openings. These openings allow the electrons that tunnel across the energy barrier to escape without losing momentum due to collisions in the cathode layer. If the cathode

layer does not have openings, then the electrons that tunnel must have sufficient momentum (energy) remaining after the tunneling to escape through the thin layer of cathode material. By having openings, electrons that tunnel that have less than sufficient energy to escape the cathode layer previously can now exit through the openings. This greatly increases the number of electrons that can be emitted from the tunneling emitter. These openings also allow for photon emission because without the openings, the photons would ordinarily be absorbed into the opaque cathode layer. By allowing a wide range of tunneled electron energies to escape through the openings, the nanoholes in the cathode layer help to reduce spiking in the emission output and improves the emission stability. Below is a Figure from Exhibit C which exhibits the nano hole structure in a 75 Angstrom gold cathode layer.



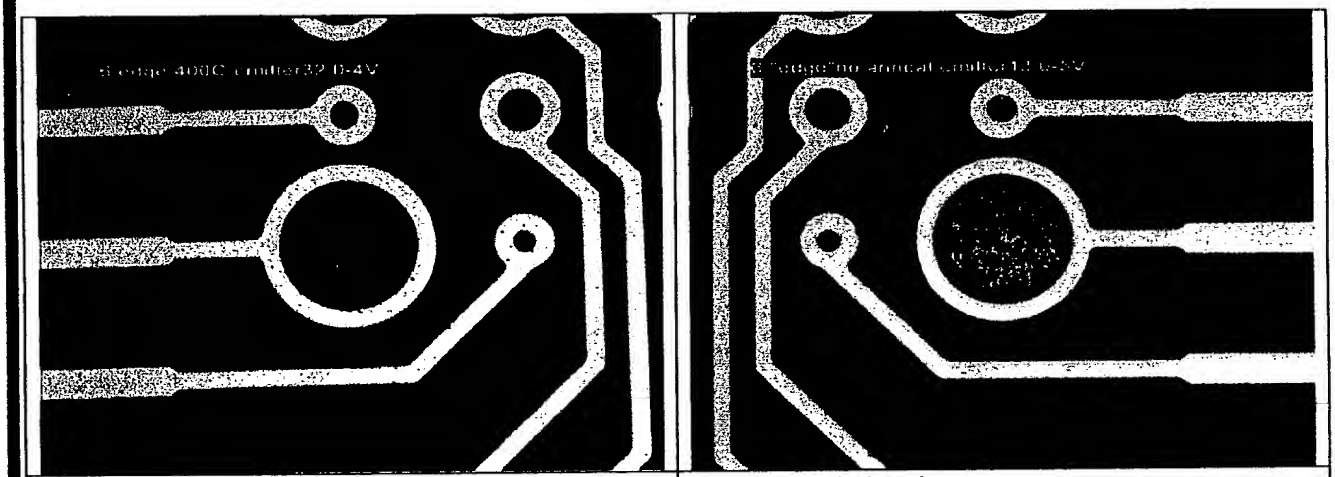
Portion of Exhibit C – Electron Microscope Picture of Nanohole Structure in Gold Cathode Layer

5) Another unexpected property that is described in the disclosure is that that an emitter processed by the annealing process can provide photonic

emissions as well as electron emissions. Below is an extract of Exhibit A, which demonstrates the photonic emission capability of the emitter.

Many researchers have point out the correlation between electron emission and light emission. Some of useful information can be found from the light emission measurements. The light emission measurements were done for annealed and non annealed emitter, respectively. The results are shown in Figure 5. It can be seen that a relative uniform light emission pattern produced by annealed emitter comparing to non annealed emitter. Also it should be pointed out that in order to clearly show the light emission from non annealed emitter high voltage is needed. For example, the light emission can be measured clearly with 4 V for annealed emitter, while 5V had to be applied to the non annealed emitter, as shown in Figure 5. Again, it showed that the effective field on annealed emitter is higher than non annealed emitter. Figure 5 also indicated a better interface, less hot spots for annealed emitter comparing non annealed emitter.

From Figure 4 and 5, it may conclude that with annealing, device series resistance is reduced and effective field is increased, also relative uniformed interface is produced.



Annealed emitter	Non- annealed emitter

Figure 4. Annealing effect on light emission pattern

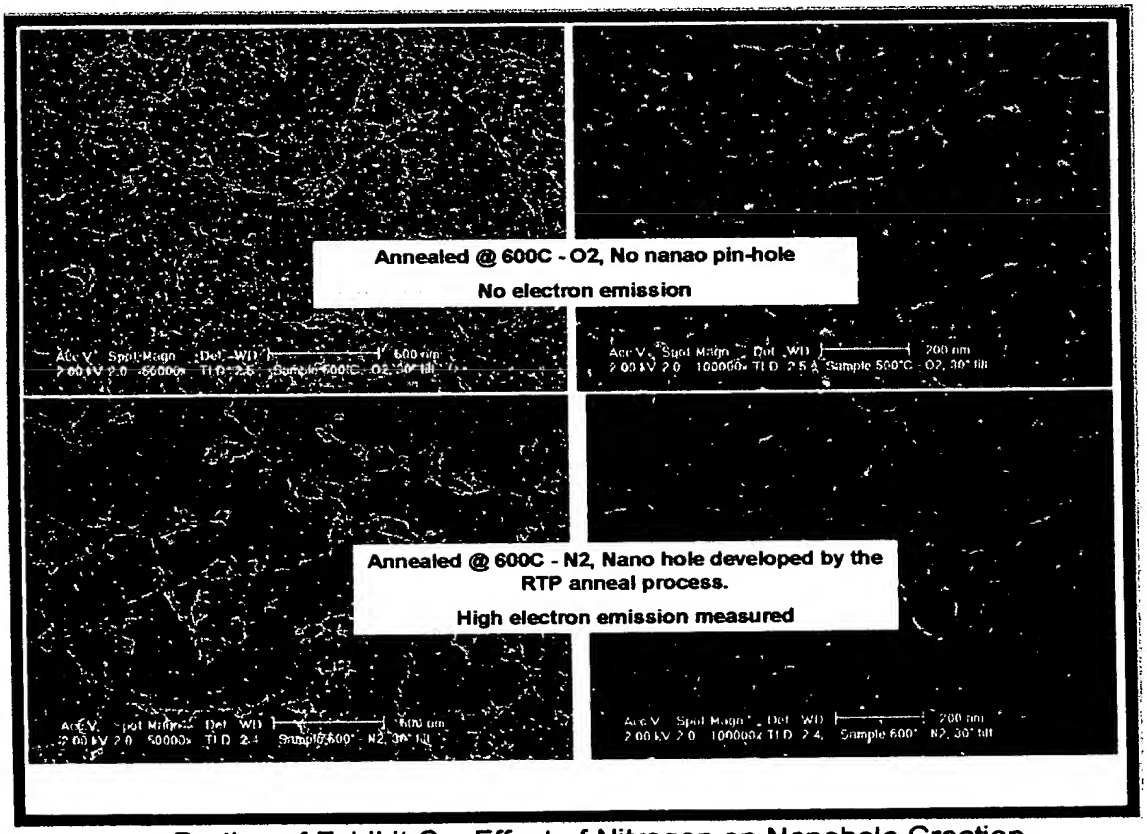
Portion of Exhibit A – Post and Pre Annealed Emitter Demonstrating Photonic Emission

It is still not completely known how the nanoholes are forming that create the openings to allow for the photons to escape. One theory is that during the annealing process, nitrogen in the ambient air is chemically attracted to the metal in the metal cluster dielectric and an oxynitride material is formed at the interface of the tunneling layer and the cathode layer. This adsorption of the nitrogen by the tunneling layer is probably also causing the cathode layer to form the pinholes due to the change in the crystalline structure which allows the metal cathode's

surface tension to pull back the metal, thereby creating openings. Its possible that the adsorbed nitrogen further acts as an impurity in the tunneling layer thus causing the decrease in tunneling resistance that characterizes the annealed emitter.

Subsequent tests (see Exhibit C) have shown that when the emitter is annealed in an only oxygen or only argon environment the nano-holes are not formed. However, nanoholes are formed when annealing is performed with either an air (which contains 78% nitrogen, 21% oxygen) or a nitrogen only atmosphere. Thus, it appears that tunneling layer undergoes a transformation during annealing by introducing impurities of nitrogen into the tunneling layer. Furthermore, the cathode layer is physically changed during annealing to create a layer with nano-sized holes that allow for increased electron and photon emissions.

Below is a Figure from Exhibit C which demonstrates the results of annealing a ~70 Angstrom platinum cathode layer in O_2 in which nanoholes where not formed and annealing a ~70 Angstrom platinum cathode layer in N_2 in which the nanoholes were formed.

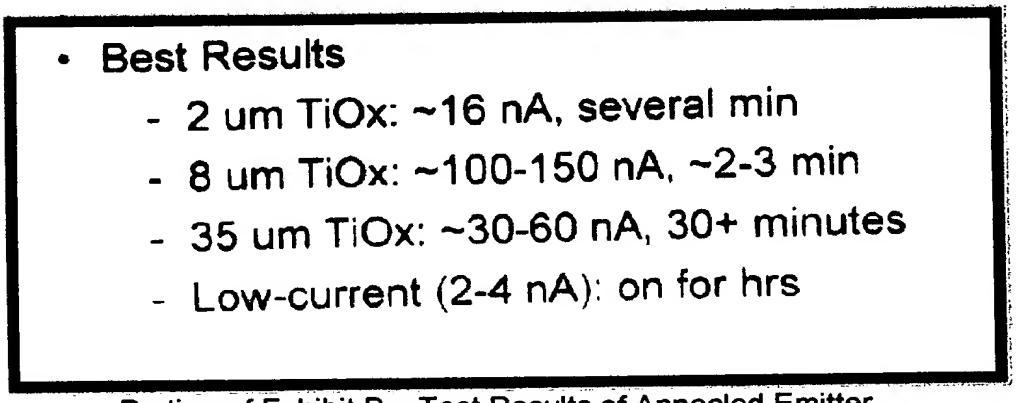


Portion of Exhibit C – Effect of Nitrogen on Nanohole Creation

It is evident that these differences in physical properties due to annealing the emitter lead to a novel structure different from that described in the prior art. As evidence of the novel structure, the change in the electrical properties of the tunneling layer and the characteristics of emission produce unexpected results in the form of increased emissions, photonic emissions, and more stable emissions which make the claimed invention unobvious over the prior art. Further evidence is the electron microscope pictures showing the nanohole formation that alters the structure of the cathode layer. In addition, characterization tests of the tunneling layer show that the tunneling resistance is decreased after annealing.

Determining whether the results are truly unexpected is addressed in the MPEP in §716.02. According to MPEP 716.02, a greater than expected result is an evidentiary factor pertinent to the legal conclusion of obviousness. Evidence of a greater than expected result may be shown by demonstrating an effect which is greater than the sum of each of the effects taken separately. The evidence should establish that the differences in result are in fact unexpected and unobvious and of both statistical and practical significance.

Below is an extracted table of best test results from the key learnings portion of the MIS Update in Exhibit B.



Portion of Exhibit B – Test Results of Annealed Emitter

The current density can be calculated based on the emitter size and the emission current. The emitter size reported is the diameter of the emitter in microns. The emission current reported (I_e) is in units of nanoamperes. Thus the current density in terms of Amps/cm^2 is:

Current density in Amps/cm^2 = I_e Amps/(10000 cm^2/m^2*3.14*(1/2*emitter size in meters)^2)

For the 2um TiOx with 16nA, this emitter has a current density of:
16E-9 Amps/(10000*3.14*(1/2*2E-6)^2) = 0.510 Amps/cm^2

For the 8um TiOx with 150nA, this emitter has a current density of:
150E-9 Amps/(10000*3.14*(1/2*8E-6)^2 = 0.299 Amps/cm^2

For the 35um TiOx with 60nA, this emitter has a current density of:
60E-9 Amps/(10000*3.14*(1/2*35E-6)^2 = 0.006 Amps/cm^2

During typical operation, these emitters will be pulsed with extremely small duty cycles, thus allowing for increased emissions due to less localized heating. By having less localized heating, the leakage current is reduced and there is less vibrations in the materials of the tunneling and cathode layers. These lower vibrations will allow more electrons to escape rather than be deflected or adsorbed. It is expected that emission currents from this low duty-cycle pulsed operation will be substantially higher, such as two to four times that measured. Therefore, these results support the claimed ranges of Applicants invention of providing an emission current of at least 10 mAmps/cm^2, 100 mAmps/cm^2, or even 1 Amp/cm^2 which are orders of magnitude greater than that accomplished by the prior art devices. These are truly unexpected results of both statistical and practical significance (see MPEP 716.02(b)), principally created by the nanohole structure in the cathode layer and lowering of the tunneling resistance created by the annealing process. Both the emission results and the structural changes to the emitter due to the annealing process are evidence of unexpected results and evidence of non-obviousness over the prior art. As noted by MPEP 716.02(d), the

"objective evidence of nonobviousness must be commensurate in scope with the claims which the evidence is offered to support."

Further with respect to the rejection of claim 1, the Applicants believe the Examiner is incorrect in citing Simmons as a reference. It is improper to use Simmons as a reference as Simmons does not disclose "an emitter" as Applicants are claiming. Simmons discloses a tunneling transistor device and not an emitter device and is incapable of electron or photonic emissions. Simmons discloses using resonant tunneling to create a negative resistance device. Simmons does not disclose, teach, or suggest using this negative resistance device as an emitter. Accordingly, the use of Simmons as a 102 reference is improper and the rejection should be withdrawn.

Applicants believe that they have demonstrated the non-obviousness of the claimed emitter and that the subjecting the claimed emitter to an annealing process creates both statistically and practical significant results which where previously unknown to those skilled in the art and therefore not disclosed, taught, or suggested by the art made of record. Further, the Applicants have demonstrated that the physical structure of the product by process emitter is different from that of the cited art. Accordingly allowance of claim 1 is respectfully requested.

In Section 14 of the Office Action, the Examiner rejected claims 2-4 under 35 USC 103(a) as being unpatentable over Simmons et al. in view of Potter. Claims 2-4 are believed patentable based at least on the patentability of claim 1 for the reasons describe above. Further, there are additional limitations which impart patentability to these dependent claims, some of which will now be discussed.

In regard to claims 2-3, the Examiner states that Simmons fails to disclose that the tunneling layer is a metal cluster dielectric, but that Potter discloses layer of alloys of titanium and tungsten and it would be obvious . . . to modify the semiconductor device of Simmons to include layer of alloys of titanium and tungsten as disclosed in Potter. Applicants respectfully traverse the Examiner's combination. Potter is directed to a "field emission" emitter device and thus does not disclose a tunneling layer nor any material that would be used for a tunneling

layer. Potter discloses metal "conductive layers" and not "dielectric" layers that contact the blade edge 100 and these are not a "tunneling layer" of "metal cluster dielectrics" which Applicants are claiming. Potter uses these metal conductive layers to indeed provide good ohmic contact to the field emissive blade edge 100. Contrarily, the Applicants are sandwiching a "metal cluster dielectric," an insulator, between the cathode layer and the electron source to create a "tunneling layer" in which electrons quantum tunnel through with sufficient energy to allow for emission of electrons from the cathode surface. Substituting the conductive layers of Potter for Applicants' "tunneling layer" would make the Applicants' invention inoperative as the electrons would not tunnel but simply conduct through Potter's conductive layers. It is the high dielectric strength of the metal cluster dielectrics which allow for high electric fields to be present without dielectric breakdown that provide the energy for the electron tunneling which creates the electron emission. Accordingly, the combination of Simmons with Potter is improper as the combination does not create Applicants' claimed invention. Accordingly, removal of the rejection under 35 USC 103(a) and allowance of claims 2-4 is respectfully requested.

In Section 15 of the Office Action, the Examiner rejected claims 5-7 under 35 USC 103(a) as being unpatentable over Simmons in view of Chuman. The Examiner states that Chuman discloses an emission device that has an emission current greater than 1×10^{-6} Amps/cm^2 and that it would be obvious . . . to modify the semiconductor device of Simmons to include an emission current greater than 1×10^{-6} Amps/cm^2 because it aids in providing high luminance. Applicants respectfully traverse the combination of Simmons and Chuman and the Examiner's assertion of obviousness. As discussed previously, Simmons is not an emitter and thus there is no motivation to increase its emissions because it doesn't have any. Further, the claimed emission is expressed in terms of current density per area. It would not be obvious to increase the emissions of Chuman, as one could not increase the current density per area by simply making the emitter larger. The Applicants have increased the emission current density by subjecting the emitter to an annealing process that changes the structure of the emitter, thus allowing for higher emissions. Indeed, Chuman shows in its Fig. 2a maximizing of current density output of about 1×10^{-3} Amps/cm^2 by manipulating

the tunneling layer thickness. The Applicants have been able to far exceed this disclosed current density by at least one order of magnitude (a factor of 10X) and indeed by even exceeding 3 orders of magnitude. In making the combination obvious, the Examiner does not disclose how one skilled in the art would increase the current density nor does Simmons or Chuman disclose, teach, or suggest a current density greater than 1×10^{-3} Amps/cm^2. If the Examiner continues to assert this rejection, the Applicants respectfully request the Examiner to provide an affidavit describing how to do so or to supply a reference.

The Applicants have disclosed and claimed how to increase the current density by using an annealing process and its ability to respectively alter the structure of the emitter by lowering the tunneling layer resistance, reducing ohmic contacts, and most importantly, creating nanohole openings in the cathode layer. It is through the application of the annealing process that these unexpected results have been obtained. None of these changes in structure have been disclosed, taught, or suggested by the proposed combination or other art made of record. Further evidence of the state of the art in electron emission density is found in Kusunoki on page 1667 (bottom of left column) wherein the emission current to date (8/20/99 when manuscript received) is 50×10^{-6} Amps/cm^2. The desire for at least 1 mA/cm^2 is noted. In Fig. 5, Kusunoki only discloses an emission density of up to this 1mA/cm^2 limit, i.e. the same as Chuman. Accordingly, the rejection under 35 USC 103(a) and allowance for claims 5-7 is respectfully requested.

In Section 16 of the Office Action, the Examiner rejected claims 8-12 under 35 USC 103(a) as being unpatentable over Simmons in view of Liu. Applicants respectfully traverse this combination. Claims 8-12 are believed patentable based at least on the patentability of their base claims. Further, both Simmons and Liu are not "emitters" as Applicants are claiming but different versions of tunneling transistors that use tunneling not to emit electrons but rather to create negative resistance. Nor does the combination disclose, teach, or suggest the limitation of subjecting the emitter to an annealing process. Accordingly, the combination of Simmons and Liu is improper and the rejection under 35 USC 103(a) withdrawn. Allowance of claims 8-12 is respectfully requested.

In Section 17 of the Office Action, the Examiner rejected claim 15 under 35 USC 103(a) as being unpatentable over Xia in view of Gibson. Applicants respectfully traverse the combination of Xia and Gibson. Claim 15 is believed patentable based at least on the patentability of claim 1 from which it indirectly depends. Further, neither Xia nor Gibson disclose an emitter having a "tunneling layer" as Applicants are claiming. Xia discloses a test device for a "field emission emitter." Gibson discloses using "field emitters" in a mass storage device. Further, neither Xia nor Gibson disclose subjecting the emitter to "an annealing process" as Applicants are claiming. Accordingly, the combination of Xia and Gibson is improper and should be withdrawn. Allowance of claim 15 is respectfully requested.

In Section 18 of the Office Action, the Examiner rejected claims 21 and 22 as being unpatentable over Moyer in view of Simmons. Applicants respectfully traverse this combination. Moyer is directed to a field emission device and does not include a "tunneling layer" as the Examiner admits. The Examiner states that it would have been obvious to use the tunneling layer of Simmons because it aids in providing a layer for electrons to travel. As stated previously, the tunneling layer of Simmons is not used for electron emission but for creating a negative resistance layer. Even so, simply adding a tunneling layer to Moyer does not disclose Applicants' structure. Applicants have the "tunneling layer formed on the electron supply layer in the opening" and "a cathode layer formed on the tunneling layer." Forming a cathode layer on the tunneling layer would defeat the purpose of Moyer which is to create an electric field that peaks in the center of the opening (see Fig. 4 of Moyer). Applicants' cathode layer is conductive and the electric field would be substantially flat across the surface of the cathode layer. Even modifying the prior art emitter shown in Fig. 1 of Moyer would change its operation from a field emitter to a tunneling emitter which operates differently. Further, neither Moyer nor Simmons, alone or in combination, disclose, teach, or suggest "wherein the emitter has been subjected to an annealing process to increase the supply of electrons tunneled from the electron supply layer to the cathode layer for energy emission." As discussed previously for claim 1, this annealing step changes the structure of the emitter such that it is different from that disclosed by Moyer and/or Simmons.

With respect to claim 22, Moyer does not disclose, teach, or suggest that the emitter is capable of emitting photons in addition to electron emission. Moyer instead teaches that the electron emitter emits electrons which strike cathodoluminescent material 22 which re-radiates energy as photons (col. 4, lines 17-31. Therefore, it is not the emitter that is emitting photons, as the Applicants are claiming, but a screen structure having cathodoluminescent material that emits the photons. Contrarily, because the Applicants have subjected the emitter to an annealing process that has changed the structure of the cathode surface to have nanohole structures, photons that are created by electron state transitions after tunneling are able to leave the emitter rather than being absorbed in the cathode layer as with conventional tunneling emitters.

Accordingly, removal of the rejection under 35 USC 103(a) and allowance for claims 21-22 is respectfully requested.

In Section 19 of the Office Action, the Examiner rejected claims 23 and 25 under 35 USC 103(a) as being unpatentable over Moyer in view of Simmons and Potter. Applicants believe that claims 23 and 25 are at least patentable based on the patentability of claim 21 from which they depend. Further, as discussed previously with respect to the rejection in Section 14 of the Office Action, Potter does not disclose using a "metal cluster dielectric" as a tunneling layer but instead using metal conductive layers which simply do not function as tunneling layers. Accordingly, withdrawal of the rejection under 35 USC 103(a) and allowance for claims 23 and 25 is respectfully requested.

In Section 20 of the Office Action, the Examiner rejected claim 24 under 35 USC 103(a) as being unpatentable over Moyer in view of Simmons and Chuman. As discussed previously for the rejection in Section 15 of the Office action, it is the anneal process that changes the structure of the emitter which allows for the higher electron density claimed by the Inventors. This annealing process is not disclosed, taught or suggested by the art made of record. The annealing process produces unexpected results which as shown provide emission current density at least one order of magnitude larger than that disclosed by previous art made of record for tunneling emitters. Accordingly, withdrawal of the rejection under 35 USC 103(a) and allowance of claim 24 is respectfully requested.

In Section 21 of the Office Action, the Examiner rejected claims 26 and 27 under 35 USC 103(a) as being unpatentable over Moyer in view of Simmons and Liu. Claims 26 and 27 are believed patentable based at least on the patentability of claim 21 from which the directly or indirectly depend. Further as discussed previously in regard to section 16 of the Office Action, it is improper to combine Simmons and Liu as neither disclose an emitter with a tunneling layer as Applicants are claiming. Further, Moyer is a field emitter and also does not disclose a tunneling emitter structure, thus Moyer in combination with Simmons and Liu do not disclose, teach, or suggest Applicants claimed invention as a whole. Accordingly, withdrawal of the rejection under 35 USC 103(a) and allowance of claims 26 and 27 is respectfully requested.

In Section 22 of the Office Action, the Examiner rejected claims 34 and 40 under 35 USC 103(a) as being unpatentable over Moyer in view of Huang and Simmons. Claim 34 has been amended to include the limitation "wherein the emitter has been subjected to an annealing process." As discussed previously, none of the art cited or made of record discloses, teaches, or suggests the Applicants' invention as a whole. Moyer is not a tunneling emitter and adding a tunneling layer within the opening does not disclose "a cathode layer disposed on the tunneling layer and portions of the conductive layer." In fact, Moyer teaches away from Applicants' claimed structure by noting that its structure of not having the cathode layer deposited in the opening in order to produce the non-uniform electric field as shown in Fig. 4 of Moyer. A person of ordinary skill in the art by simply referring to the Moyer, Huang and Simmons references would not be able to create the overall structure of Applicants' claimed invention in claim 34. Nor would the person of ordinary skill be able to create an emitter that emits photons as Applicants are claiming in claim 40. Moyer discloses using an emitter to emit electrons which strikes a display that has cathodoluminescent material that then converts the electrons to photons. The emitter of Moyer does not emit photons as Applicants are claiming. By annealing the emitter, the structure changes, in particular the cathode layer forms nanoholes, such that photon emission and increased electron emission are possible. This annealing process is not

Accordingly, withdrawal of the rejection under 35 USC 103(a) and allowance of claims 34 and 40 is respectfully requested.

In Section 23 of the Office Action, the Examiner rejected claim 35 as being unpatentable over Moyer in view of Huang and Simmons and Chuman. Claim 35 is deemed patentable based on the patentability of its parent, claim 34, as amended. Further, claim 35 is believed separately patentable. As discussed previously, Simmons is not an emitter and thus there is no motivation to increase its emissions because it doesn't have any. Further, the claimed emission is expressed in terms of current density per area. It would not be obvious to increase the emissions of Chuman, as one could not increase the current density per area by simply making the emitter larger. The Applicants have increased the emission current density by subjecting the emitter to an annealing process that changes the structure of the emitter, thus allowing for higher emissions. Indeed, Chuman shows in its Fig. 2 a maximizing of current density output of about 1×10^{-3} Amps/cm^2 by manipulating the tunneling layer thickness. The Applicants have been able to far exceed this current density by at least one order of magnitude (a factor of 10X) and indeed by even exceeding 2 orders of magnitude ("about 0.1 to about 1.0 Amps/cm^2" as Applicants are claiming). In making the combination, the Examiner does not disclose how one skilled in the art would increase the current density nor does Simmons or Chuman disclose, teach, or suggest a current density greater than 1×10^{-3} Amps/cm^2. By using the annealing process and its ability to respectively alter the structure of the emitter by lowering the tunneling layer resistance, reducing ohmic contacts, and most importantly, creating nanohole openings in the cathode layer these unexpected results have been obtained. None of these changes in structure have been disclosed, taught, or suggested by the proposed combination. Further evidence of the state of the art in electron emission density is found in Kusunoki on page 1667 (bottom of left column) wherein the emission current to date (8/20/99 when manuscript received) is 50×10^{-6} Amps/cm^2. The desire for at least 1 mA/cm^2 is noted. In Fig. 5, Kusunoki only discloses an emission density of up to this 1mA/cm^2 limit, i.e. the same as Chuman. By annealing the emitter, Applicants have significantly and substantially outperformed emitters created by prior art techniques. Accordingly,

the rejection under 35 USC 103(a) and allowance for claim 35 is respectfully requested.

In Section 24 of the Office Action, the Examiner rejected claim 36 (it is assumed that claim 35 was a typo due to the context of the rejection) under 35 USC 103(a) as being unpatentable in view of Huang and Simmons and Potter. As stated previously for Section 14 of the Office Action, Potter does not disclose, teach, or suggest where the tunneling layer is a "metal cluster dielectric" as Applicants are claiming. Further claim 36 is believed patentable based on the patentability of its parent claim, claim 34, as amended. Accordingly, the rejection under 35 USC 103(a) and allowance for claim 36 is respectfully requested.

In Section 25 of the Office Action, the Examiner rejected claims 37-39 under 35 USC 103(a) as being unpatentable over Moyer in view of Huang and Simmons and Liu. Claims 37-39 are deemed patentable based on the patentability of parent claim 34, as amended. Accordingly, the rejection under 35 USC 103(a) and allowance for claims 37-39 is respectfully requested.

The prior art made of record but not relied upon by the Examiner has been reviewed, but is no more pertinent to Applicants invention than the cited references for the reasons given above.

Applicants believe their claims as amended are patentable over the art of record, and that the amendments made herein are within the scope of a search properly conducted under the provisions of MPEP 904.02. Accordingly, claims 1-17 and 21-40 are deemed to be in condition for allowance, and such allowance is respectfully requested.

Respectfully Submitted,
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APPENDIX A

Marked-up Version of Changes

In the Specification:

Fig. 2 is an exemplary diagram of a use for the emitter 50 of Fig. 1. In this application, the electron emission 16 is focused by an electrostatic focusing device or lens 28, exemplified as an aperture in a conductor that is set at predetermined voltage 36 that can be adjusted to change the focusing effect of the lens 28. Those skilled in the art will appreciate that lens 28 can be made from more than one conductor layer to create a desired focusing effect. The electron emission 16 is focused by lens 28 into a focused beam 32 onto an anode structure 30. The anode structure 30 is set at an anode voltage V_a 26 which magnitude varies for an application depending on the intended use and the distance from the anode structure 30 to the emitter 50. For instance, with anode structure 30 being a recordable medium for a storage device, V_a might be chosen to be between 500 and 1000 Volts. The lens 28 focuses the electron emission 16 by forming an electric field 34 within its aperture. By being set at a proper voltage from V_e, the electrons emitted from the emitter 50 are directed to the center of the aperture and then further attracted to the anode structure 30 to form the focused beam 32.

In the Abstract:

An emitter has an electron supply layer and a tunneling layer formed on the electron supply layer. Optionally, an insulator layer is formed on the electron supply layer and has openings defined within [in]which the tunneling layer is formed. A cathode layer is formed on the tunneling layer to provide a surface for energy emissions of electrons and/or photons. Preferably, the emitter is subjected to an annealing process thereby increasing the supply of electrons tunneled from the electron supply layer to the cathode layer.

In the Claims:

1. (Amended) An emitter, comprising:

an electron supply;

a cathode layer; and

a tunneling layer disposed between the electron supply and the cathode layer wherein the electron supply, cathode layer, and tunneling layer have been subjected to an annealing process.[.]

7. (Amended) The emitter of claim 1 operable to provide an emission current of greater than 1×10^{0} Amps per square centimeter.

34. (Amended) An emitter, comprising:

an electron supply surface;

an insulator layer formed on the electron supply surface and having a first opening defined within;

an adhesion layer disposed on the insulator layer; the adhesion layer defining a second opening aligned with the first opening;

a conductive layer disposed on adhesion layer and defining a third opening aligned with the first and second openings;

a tunneling layer formed on the electron supply layer within the first, second, and third openings; and

a cathode layer disposed on the tunneling layer and portions of the conductive layer, wherein the portion of the cathode layer on the tunneling layer is an electron-emitting surface wherein the emitter has been subjected to an annealing process.

Appendix B
Exhibits

Exhibit A – "Direct Tunneling Emitter Process Development and Improvement," dated 1/12/2001. This status report describes the differences observed between annealed and unannealed emitters.

Exhibit B – "MIS Update – Planfest IV," dated 3/20/2001. This status report on testing and failure analysis of the metal cluster emitters lists the results of electrical testing on emission currents.

Exhibit C – "Nano Holes in Thin Metal Layer – A Key for the Electron Emission for Flat Emitter Device," undated. This slide presentation shows the changes in the cathode layer due to the affects of annealing the emitters.

Exhibit D – "Emitter Energy Testing," undated. This slide shows the test setup used to measure the diode and emission currents to better understand how the results listed in Exhibit B were obtained.

HP Company Confidential

To: Lori Tully, Paul Benning, James Smith, Tom Novet, David Schut, Bao Yeh, Mike Regan, Paul Harmon, Paul McClelland, David Pidwerbecki, John Bamber, Tim Myer, Jim Brug, Steve Naberhuis, Hueipei Kuo, Sity Lam, Henryk Birecki, Paul Cooperrider,

CC: JP Whitlock, Cathy Peltier, Clint Zlatnik, Tim Koch, Thomas Lindner, Laura king, and Jim McMahon

From: John Chen, Sriram Ramamoorthi, Mark Johnstone, Brian Bolf, Todd Berdahl, Terry McMahon, David Neiman

Date: 1/12/2001

Direct tunneling emitter process development and improvement

Summary

Three major process changes have been made since the first cycle of learning on direct tunneling emitter. First, Pt dry etch process was developed to replace the oxide trench etch to resolve emitter isolation issue; Secondly, a dielectrics lift-off process was developed and process flow was redesigned so that emission layer was deposited after first layer metal etch to effectively prevent top to bottom electrode shorting; Third, an annealing process was implemented to improve device yield and emission test. The experiments showed that by using this improved process, the isolation between emitters and top to bottom electrode shorting became no issue, and annealing process improves device performance significantly. Comparing with non annealed process, annealed emitters make emission last longer and more repeatable, and device yield increases to 40 % from 12.5%.

Significant improvements were made, some of major challenges, however, are still ahead, such as low emission current density (~ 0.1 A/cm2 is the current density measured, 1 A/cm2 is the goal), emission flickering, and we also need to show focusing capability on MIS emitter device. These issues will be the main focus for our next move.

Process integration

Two cycles of learning on fabrication process of direct tunneling emitter were summarized in this report. The first cycle was served as process debug for unite process and whole process flow as well. The first cycle of direct tunneling process and structure is shown in Figure 1. There were two major issues we learn from the first cycle: 1.Emitter to emitter (or pad to pad) isolation issue; and 2. top to bottom electrode shorting. Failure analysis showed that the root cause of isolation failure between emitters is the results of combination of insufficient oxide trench and better than expected step coverage from Pt deposition. The top to bottom electrode shorting was caused by insufficient etch selectivity of Ta etch process, which is very difficult to achieve for the tunneling thin films we are using. Because of these issues, the pad to pad resistance was measured ~ 10 Ohms, and top to bottom electrode resistance is less than 100 Ohms.

Major process steps in first cycle

1. Define emission area by FOX
2. Emission layer deposition
3. Ta/Au (500 A/2000 A) deposition
4. Metal 1 photo patterning
5. Au wet etch
6 Ta dry etch
7. Trench photo
8. Oxide trench etch
9. Top thin metal deposition (50 – 100 A)

With Pt etch process the emitter isolation improved significantly. The emitter with Pt etch isolation was shown in Figure 3, where emitter area before and after the Pt etch isolation were shown. The test showed that this isolation is very effective. The pad to pad resistance increased from ~10 Ohms with oxide trench isolation to a typical value greater than 30 M-Ohms with Pt etch isolation. In most measurements, the resistance value is out of measurement range.
A dielectrics lift-off process was developed and process flow was redesigned so that emission layer was deposited after first layer metal etch to effectively prevent top to bottom electrode shorting. With this process flow change and the dielectric layer lift-off process, the very high selectivity requirement for metal etch is no longer needed. The top to bottom shorting was prevented effectively, and it become no issue.

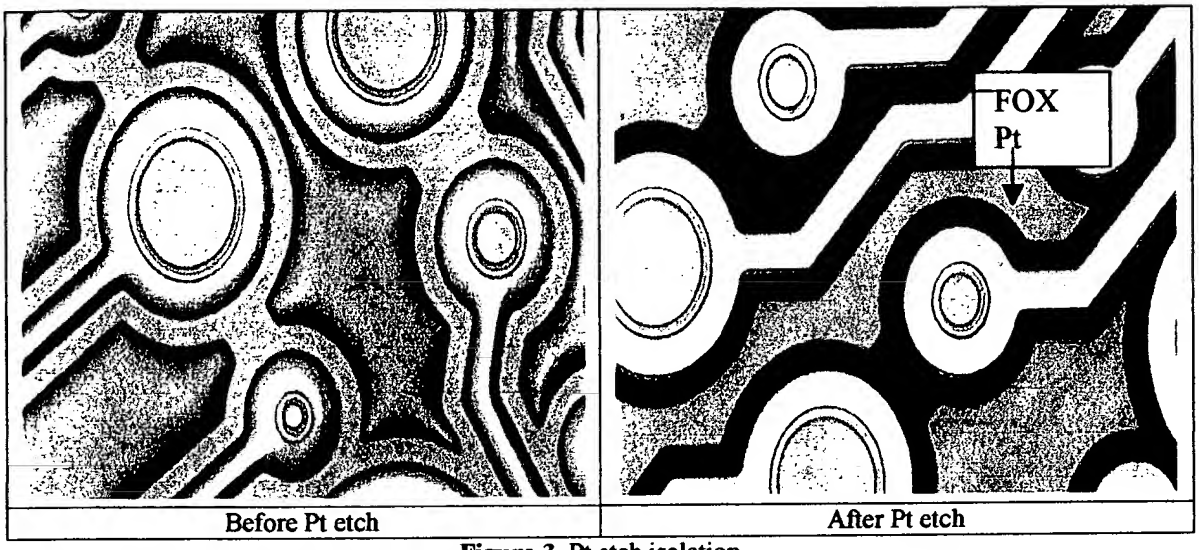


Figure 3 Pt etch isolation

Annealing Effects

Annealing experiments were done at two different conditions 400 C and 600 C, all with N2 purge and with 20 min duration. The annealing was done in a RTP system with no vacuum capability. The annealing conditions were shown in Figure 4 for both 400 C and 600 C anneal.

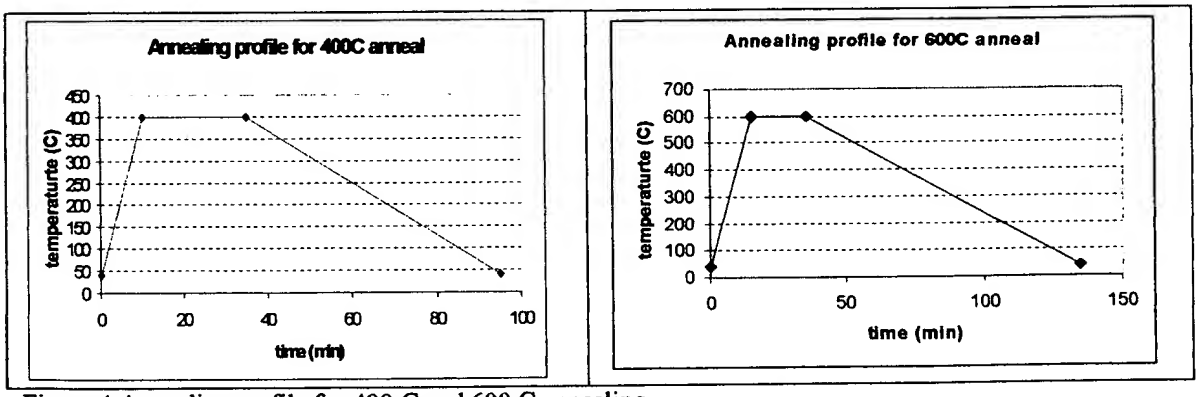


Figure 4 Annealing profile for 400 C and 600 C annealing.

A comparison of emission result between annealed and non-annealed emitter were shown in Table 1. More detailed emission result can be found from David Pidwerbecki's presentation (1/8/2001). Comparing with non annealed process, the annealed emitters make emission longer (last about minutes, instead of seconds from non annealed emitter), and most of all, the annealed emitters make repeatable emission test for the first time, and device yield increases to 40 % from 12.5%. In this set of experiments, the 400 C anneal gave a better emission results, as shown in Table 1.

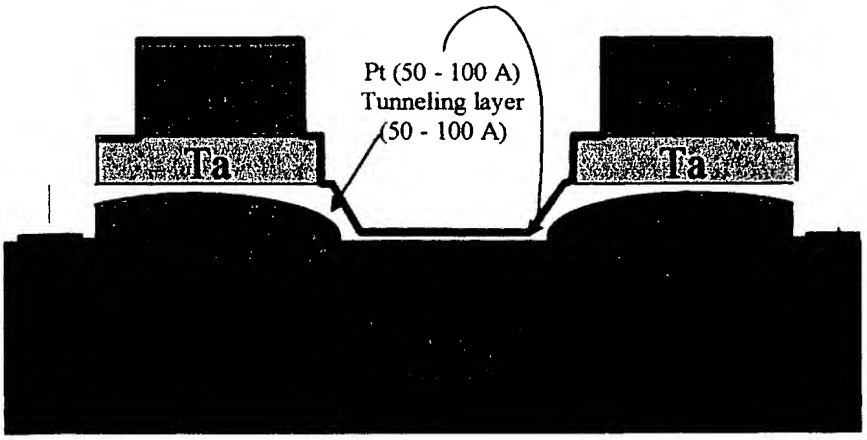


Figure 1. First generation of direct tunneling emitter design.

The second cycle of experiments were initiated to address the isolation and shorting issues. Three major changes were made. First, Pt dry etch process was developed to replace the oxide trench etch to resolve emitter isolation issue; Secondly, a dielectrics lift-off process was developed and process flow was redesigned so that emission layer was deposited after first layer metal etch to effectively prevent top to bottom electrode shorting; Third, an annealing process was implemented to improve device yield and emission test. The major process steps and structure were designed as shown in figure 2.

Improved process flow and major steps

1. Define emission area by FOX
2. Ta/Au (500 A/2000 A) deposition
3. Metal 1 photo patterning
4. Au wet etch
5 Ta dry etch
6. Tunneling layer dep./lift off
7. Top thin metal dep. (50 A – 100 A)
8. Trench photo
9. Thin metal etch (or lift-off)
10. Anneal

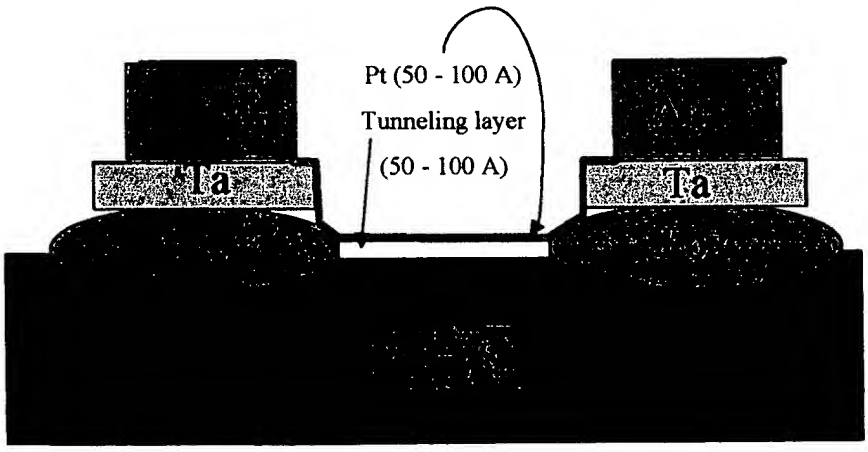


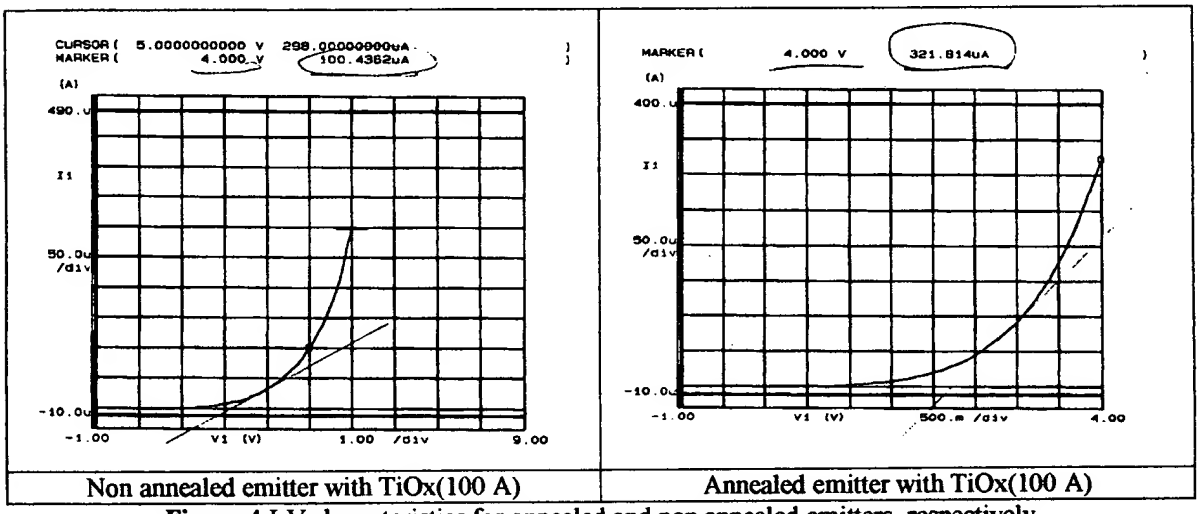
Figure 2 Improved structure to provide good isolation and prevent top to bottom electrode shorting.

Table 1. Summary of emission results for different emission film and annealing conditions.

Emission material (thickness)	Wafer ID	# emitter tested	# emitter emitted	Yield (%)	Emission repeatable	Anneal
WSiN(50)	E1	8	1	12.5	No	No
WSiN(50)	C1	8	0	0		No
WSIN(100)	E3	40	4	10	No	No
WSiN(100)	C3	8	0	0		No
TiOx(50)	E5	32	0	0		No
TiOx(50)	C5	32	0	0		No
TiOx(100)	E6	8	1	12.5	No	No
TiOx(100)	C6	21	0	0		No
WSiN(50)	E1-600C	35	10	29	Yes	Yes-600C
TiOx(100)	E6-600C	35	7	20	Yes	Yes-600C
TiOx(100)	E6-400C	35	14	40	Yes	Yes-400C

Note: E-wafer edge; C-wafer center.

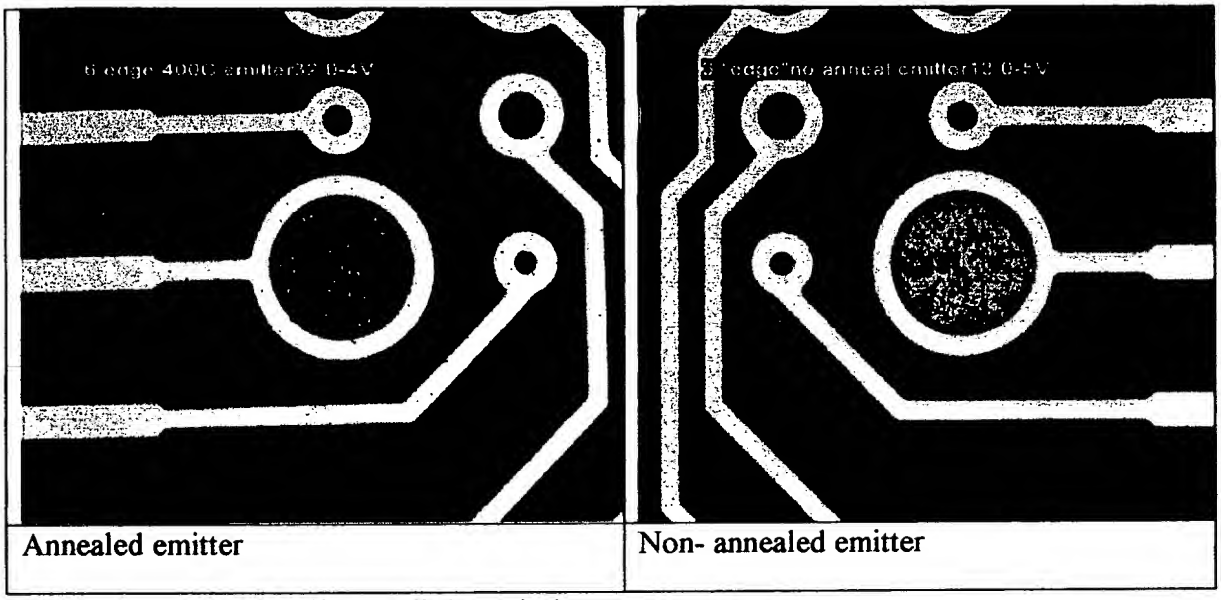
Some analyses were done to understand the effect of annealing. Figure 4 showed the I – V characteristics for annealed and non annealed emitter, respectively. It showed that at a fixed voltage, the tunneling current for the annealed emitter is about 3 time higher than non annealed emitter. If we took the slope of voltage versus current, we found that the device series resistance for annealed emitter is 3 times lower than non annealed emitter. Therefore, it suggests that the effective electric filed to enhance tunneling is higher for annealed emitter than for non annealed emitter at given voltage.



Non annealed emitter with TiOx(100 A) | Annealed emitter with TiOx(100 A)

Figure 4 I-V characteristics for annealed and non annealed emitters, respectively

Many researchers have point out the correlation between electron emission and light emission. Some of useful information can be found from the light emission measurements. The light emission measurements were done for annealed and non annealed emitter, respectively. The results are shown in Figure 5. It can be seen that a relative uniform light emission pattern produced by annealed emitter comparing to non annealed emitter. Also it should be pointed out that in order to clearly show the light emission from non annealed emitter high voltage is needed. For example, the light emission can be measured clearly with 4 V for annealed emitter, while 5V had to be applied to the non annealed emitter, as shown in Figure 5. Again, it showed that the effective field on annealed emitter is higher than non annealed emitter. Figure 5 also indicated a better interface, less hot spots for annealed emitter comparing non annealed emitter.
From Figure 4 and 5, it may conclude that with annealing, device series resistance is reduced and effective field is increased, also relative uniformed interface is produced.



Annealed emitter	Non- annealed emitter

Figure 4. Annealing effect on light emission pattern

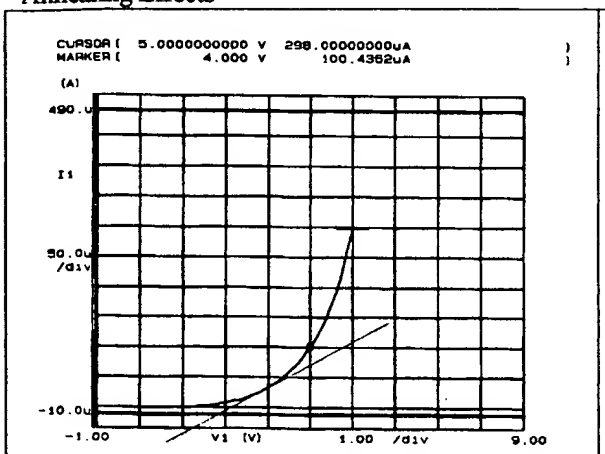
Path forward

Some of major challenges will be addressed, such as low emission current density (~ 0.1 A/cm2 is the current density measured, 1 A/cm2 is the goal), emission flickering, and focusing capability.
The optimization of emission layer thickness (thicker direct tunneling film in the rang of 100 – 250 A is planned), annealing condition (forming gas effect) , and Pt thickness control will target on low emission current and device yield improvement. Device structure and emission material modification may be needed to address the flickering issue. And two metal parts process development will address the emitter focusing capability.

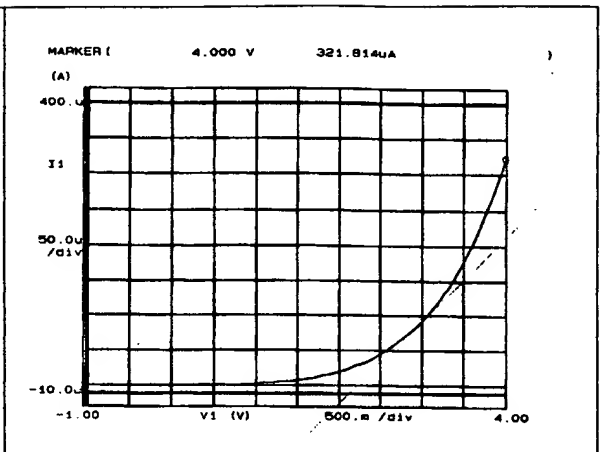
Acknowledgement

This project could not happen without support from ORCA program, especially, the strong support and inspiration from Lori Tully and Mike Regan. Special thanks to Tom Novet for his great effort and ground work in the early MIS emitter process development. Thanks to Paul Benning for many useful discussions. Thanks to David Pidwerbecki and David Schut for the emission test and communicating the results. And of course, non of this would happen without the continued managerial support of JP Whitlock, Cathy Peltier, and Clint Zlatnik from B2 fab operation.

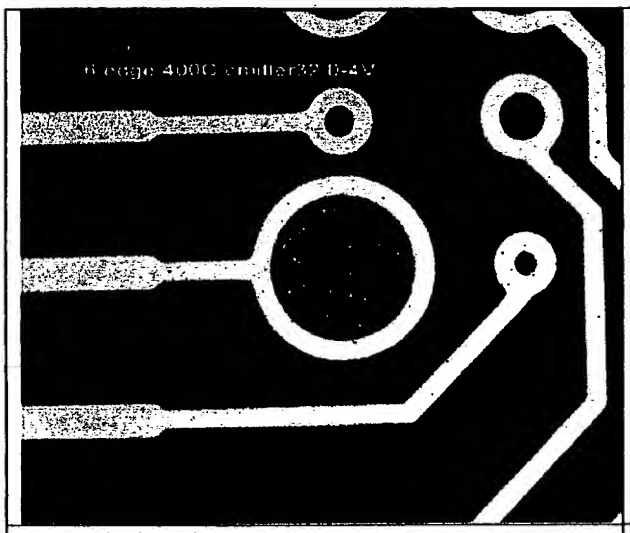
Annealing Effects



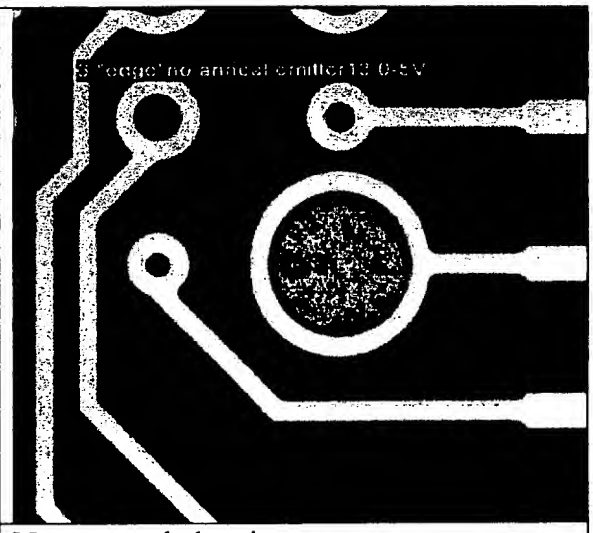
Non annealed emitter with TiOx(100 A)



Annealed emitter with TiOx(100 A)



Annealed emitter



Non- annealed emitter

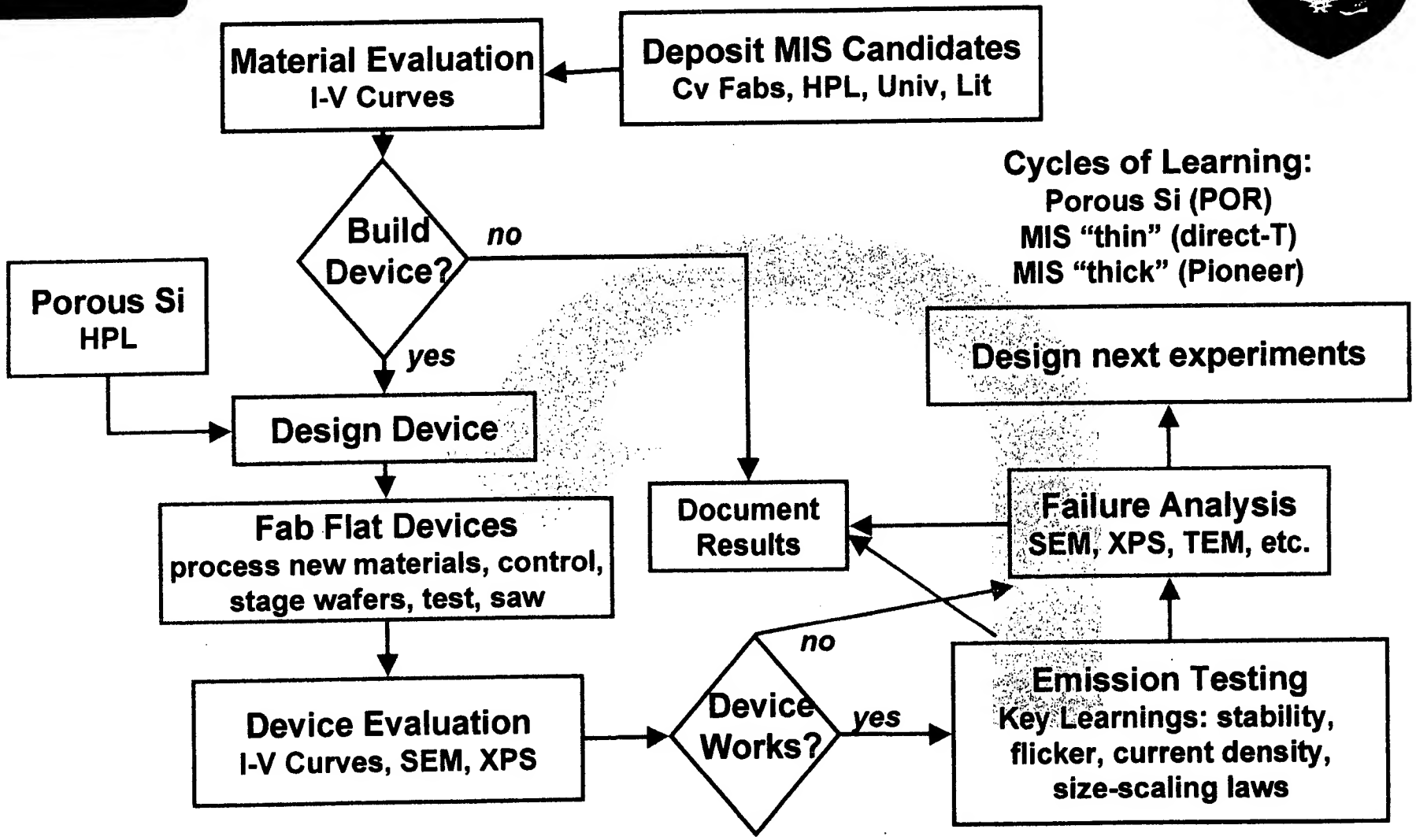
MIS Flat Emitters

MIS Update -- Planfest IV

- Flat Emitter Strategy
- Key Learnings
- Test Results / Failure Analysis
- Conclusions

MIS Flat Emitters

Flat Emitter Strategy



MIS Flat Emitters

Key Learnings (1)

- Emission test results
  - Thick emitters -- poor emission. Good Pioneer-style emitter not found -- no publications to point us in correct direction.
  - Thin direct-tunneling emitters best emission. TiOx is best to date, but not enough statistics to say for sure (TiOx is from better dep system). Thicker of "thin" materials best results.
  - The thinner the Pt (that we have studied), the better the emission.
  - Annealing improves emission properties tremendously. At 400 and 600C, much better results. Alex has developed intuitive model to explain electroforming/annealing effects.
  - Electroforming ('conditioning') is a major factor in the emitter performance. Modifies significantly the diode current and produces emission (or can kill it!)
  - Pulsing appears to have no effect over the best timescales presently measured (~1 usec)
  - No change in emission up to 2e-5 Torr with TiOx emitter

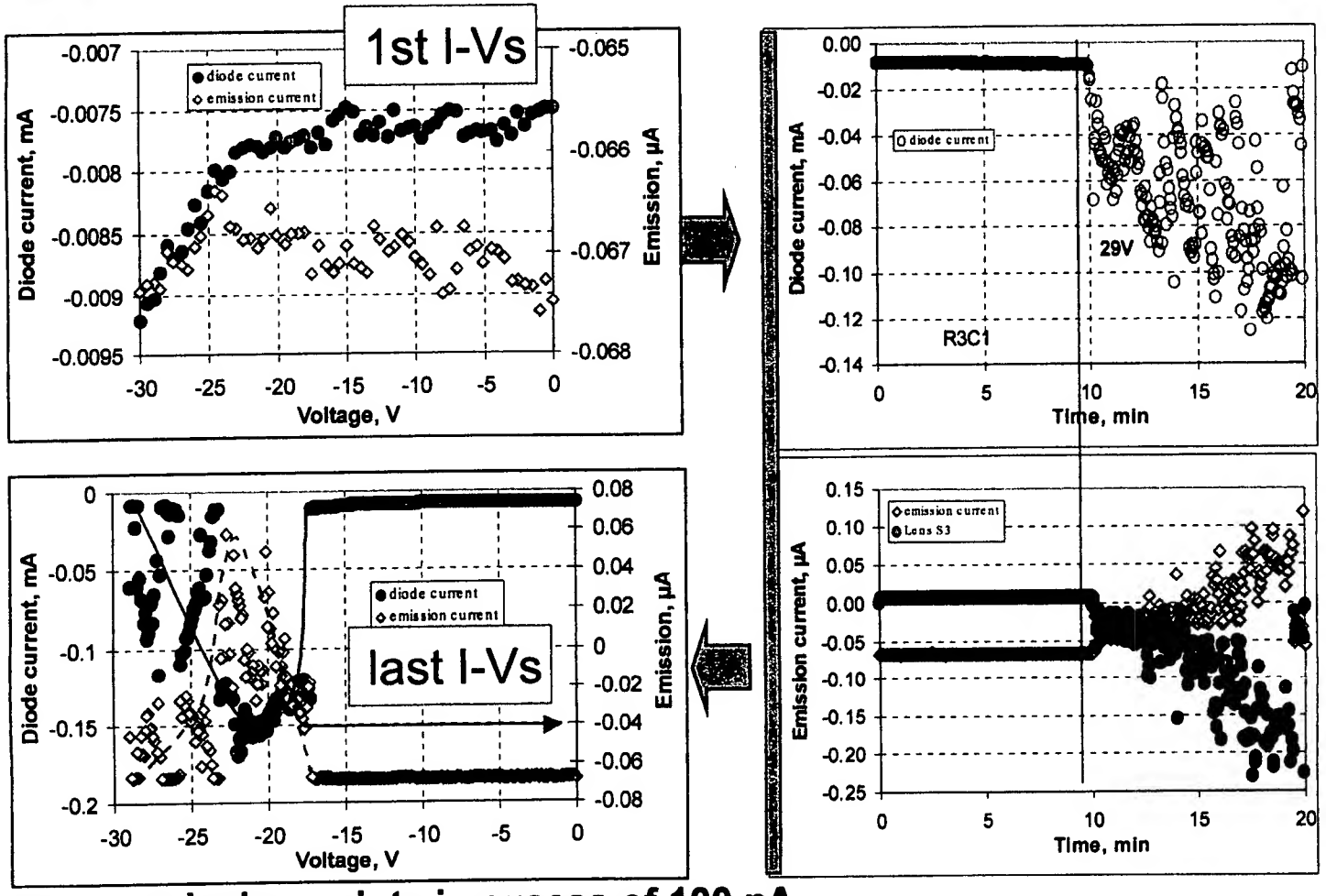
MIS Flat Emitters

Key Learnings (2)

- I-V curves tell a lot about dielectric, emitter, electrical properties device
- A lot of work remains to optimize material and thickness (dielectric and top metal). Took a lot of chances by narrowing field early
- Failure analysis tells us a lot. Good hypotheses of what is happening: non-uniform edge emission, flicker, effects of annealing
- Thermal modeling shows hot spots can exist but temperature rise is not significant. Assumes homogeneous electron transport across emitter; localized electron transport model not attempted
- Experience counts for a lot -- Alex has joined the staff
- Best Results
  - 2 um TiOx: ~16 nA, several min
  - 8 um TiOx: ~100-150 nA, ~2-3 min
  - 35 um TiOx: ~30-60 nA, 30+ minutes
  - Low-current (2-4 nA): on for hrs

MIS Flat Emitters

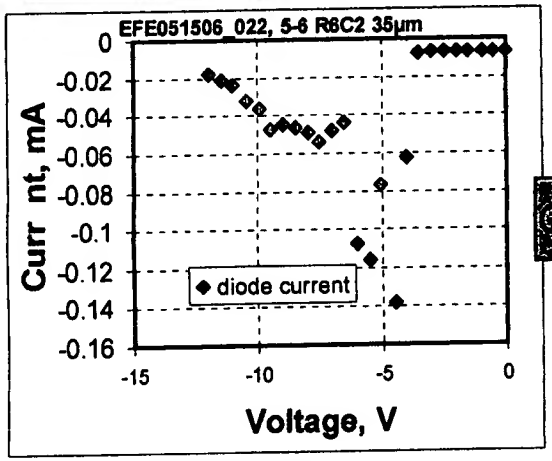
Best performance of flats #6 (DC): 8 um diameter, 10 nm TiOx, air annealed 600°C

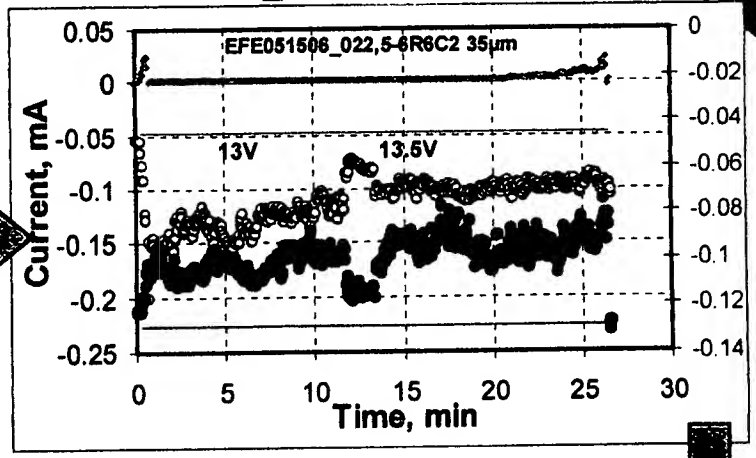


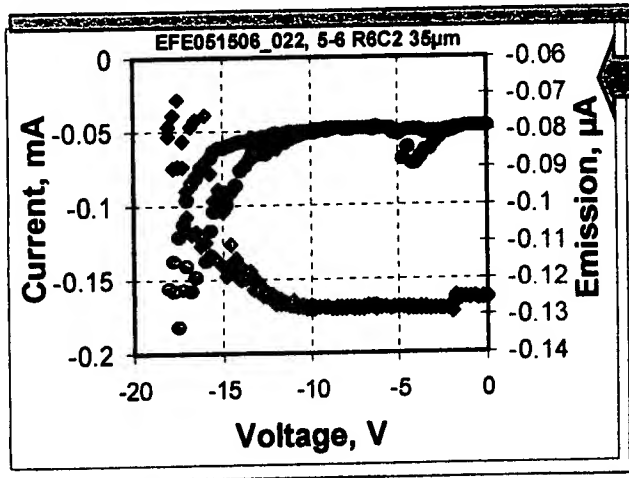
- Numerous emission points in excess of 100 nA
- Emission ramps with voltage and then collapses
- Efficiency ~ O(10E-3)

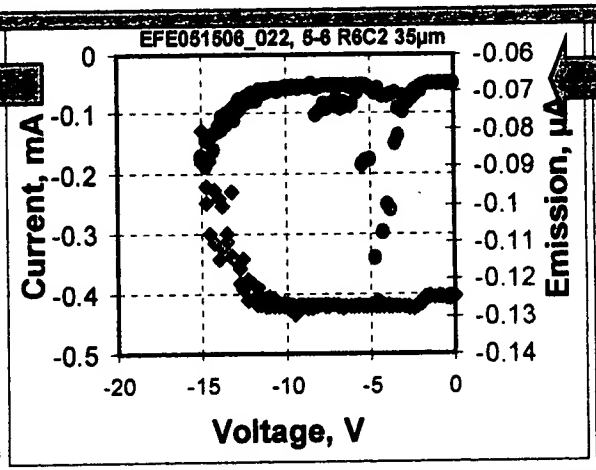
MIS Flat Emitters

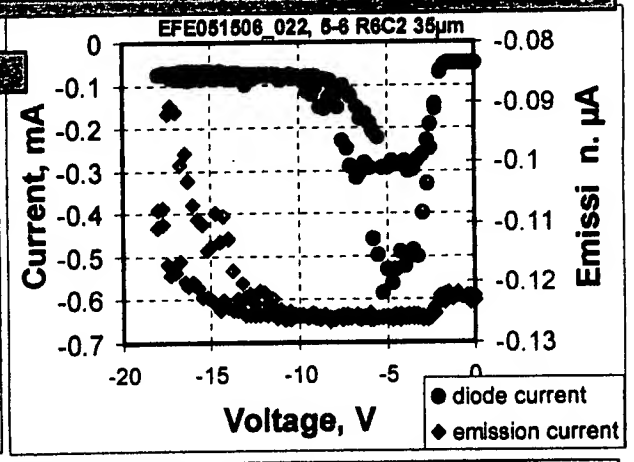
3-03-01 EFE051506_022_2-6 R9C2&R4C3
10nm TiOx 10nm Pt 600°C N_2











- Efficiency ~0,1%
- 20-60 nA emission
- >30 min (total) emission.

- Low current (~100 µA) and relatively high voltage
- Very difficult conditioning (~2 days or ~6-8 hors)
- high efficiency, edge effect

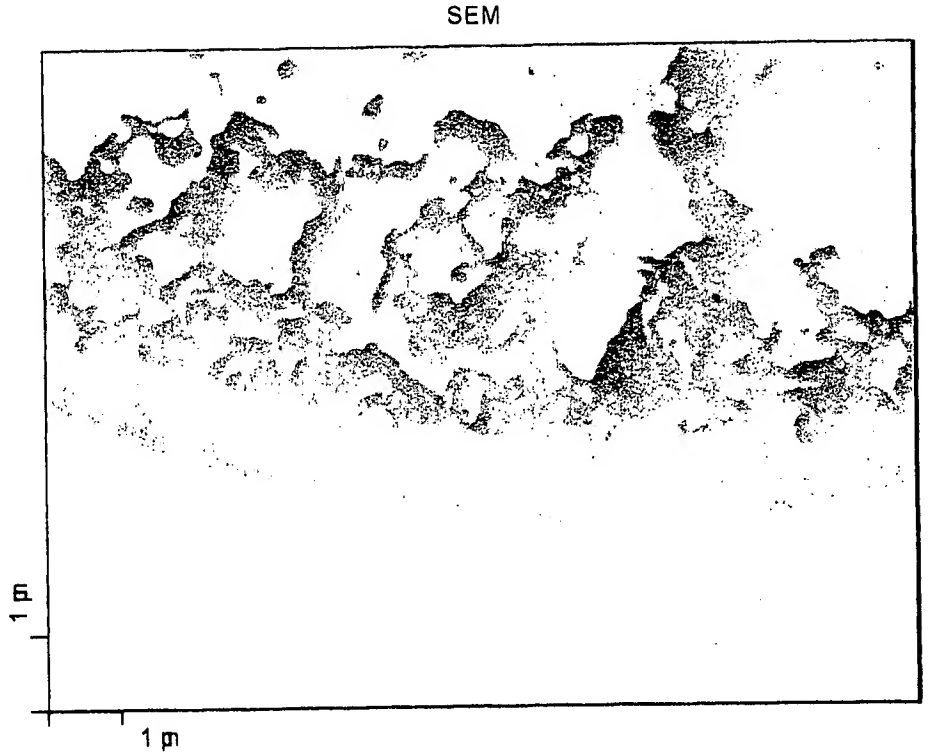
MIS Flat Emitters

Key Questions

- Why do most emitters have failure patterns at edges?
- Why is 'electroforming', annealing so important?
- Why are the emitter surfaces filled with potholes? "Beetle Gallery"

As Received

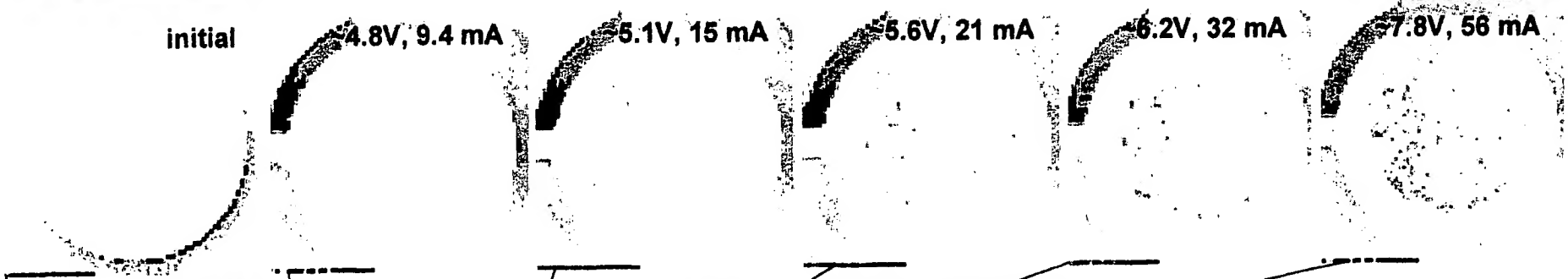
After 7.5 V Bias applied



MIS Flat Emitters

EFE037093_006, 5-3 R6C2 35µm as fabricated

Unannealed 10nm TiOx/10nmPt, SEM *in situ*



~4.8V, 9.4 mA numerous spots

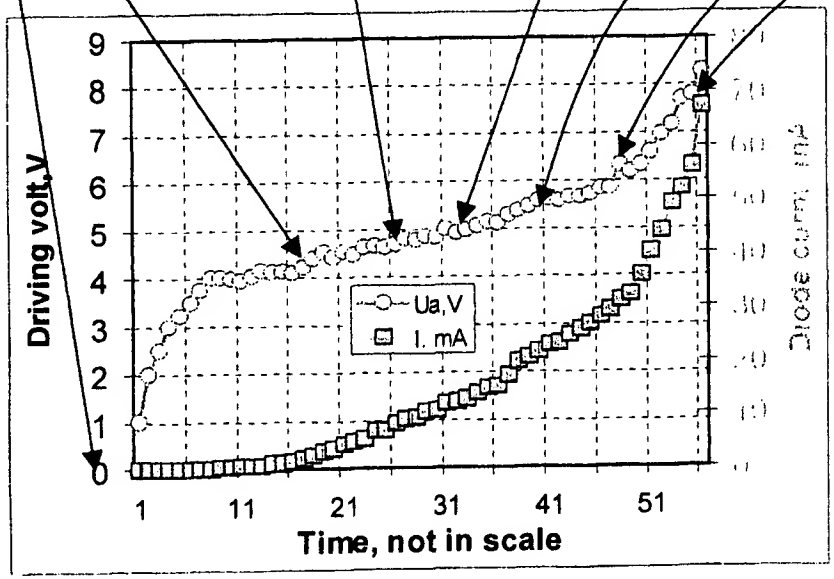
~5.1V, 15 mA numerous spots started to increase in diameter

~5.6V, 21 mA they are growing

~6.2V, 32 mA stable channels number

~7.8V, 56 mA infrequent single sparkling emission

~4.4V, 3.7 mA first two black spots appeared

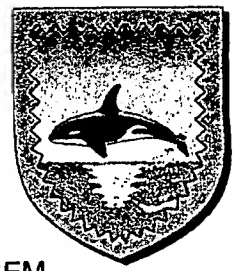


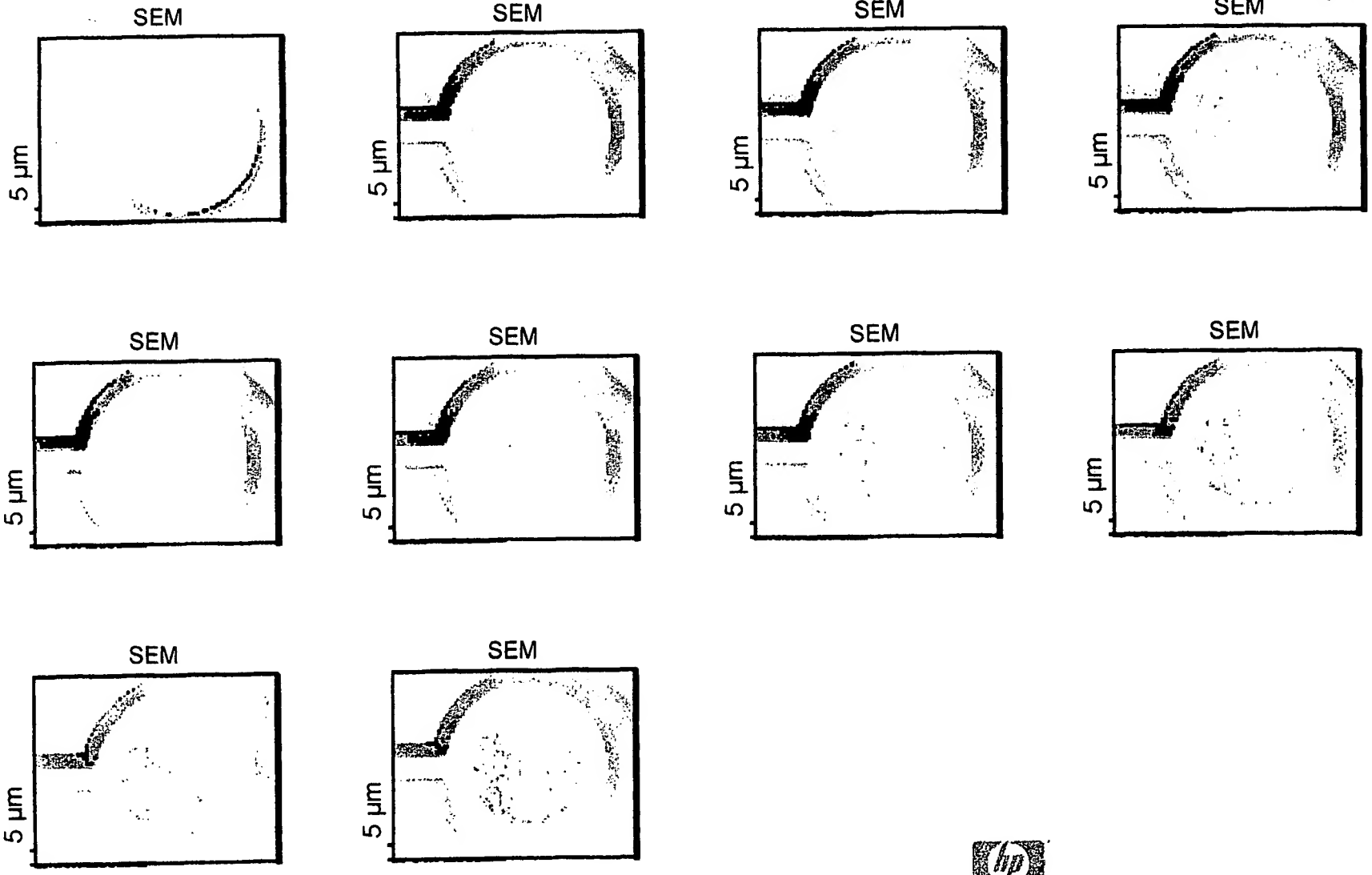
- ~uniform conditioning
- Drive 2µm emitter to get higher voltage for emission

1/21/00

MIS Flat Emitters

EFE037093-006 5-10 R6C2 no anneal





MIS Flat Emitters

EFE037093_006, R3C3 35µm 600°C Air

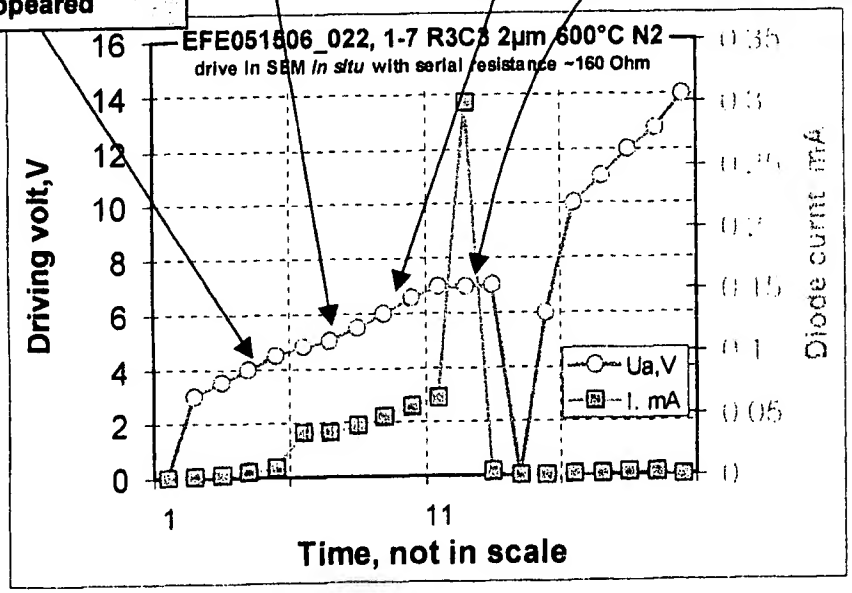
600°C in air 10nm TiOx/10nmPt, SEM *in situ*

~4.8V, 9.4 mA numerous spots

~4.4V, 3.7 mA first two black spots appeared

numerous spots started to increase in diameter

~15.5V, 0.05 mA emission 'stars' started



- Very low current and short at low voltage
- breakdown of AuTa/Pt boundary

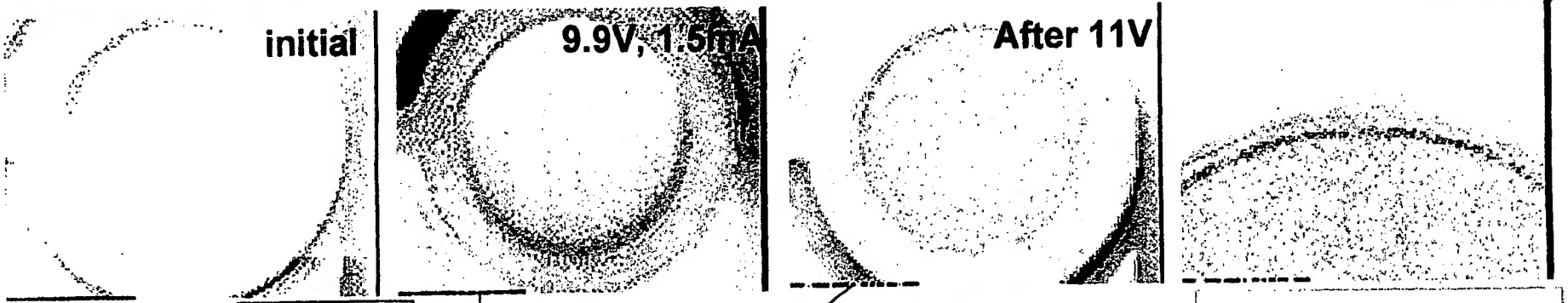
invent

1/21/00

MIS Flat Emitters

EFE051506_022, 1-7 R3C3 35µm 600°C N_2

600°C N_2, 10nm TiOx/10nmPt, SEM *in situ*



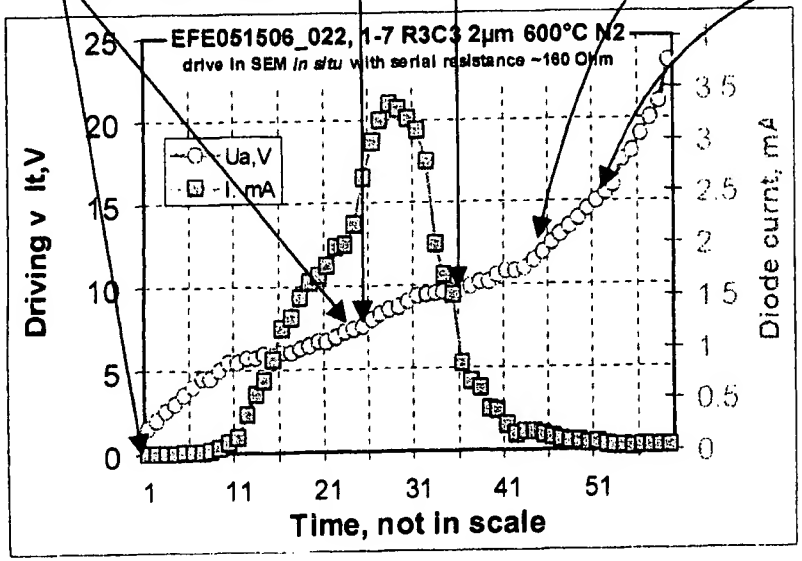
~7.7V, 2.2 mA small changes in center

~9.8V 1.6mA picture

~15.5V, 0.05 mA emission 'stars' started

~up to 7.5V, 2 mA no changes in SEM

- Low current
- High voltage performance
- FOX edge effect

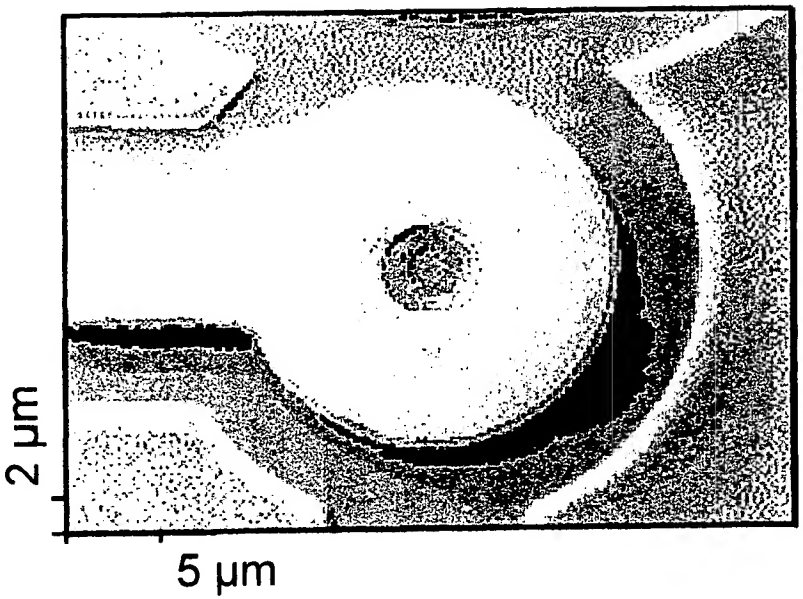


1/21/00

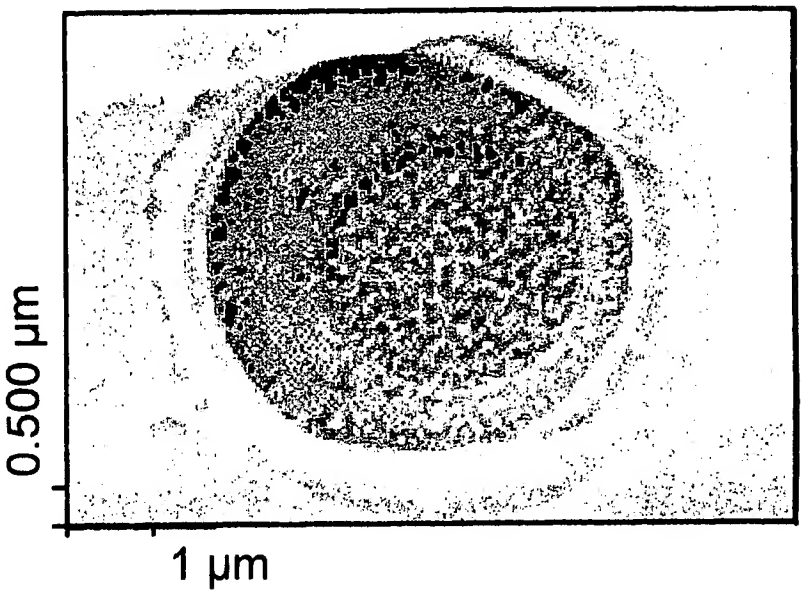
MIS Flat Emitters

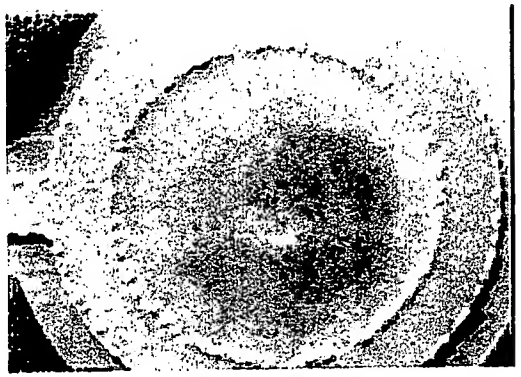
EFE037093-22 1-7 R6C1 Annealed 600°C N_2 No Emission Testing

SEM



SEM





Another sample annealed at ~750 C

MIS Flat Emitters

Model of Emission (breakdown)

- TiOx and Pt film structure critical
- Current looks for channels or low ρ "weak sites" to conduct
- Few exist, so electrons create sites
- Entire current passes through few channels, destroying Pt
- Emission continues or is quenched and looks for new weak sites
- Unannealed samples have failures across emitter surface
- Annealed samples have failures at edge due to coalescence effects

Thin Pt

Thin TiOx (as-dep)

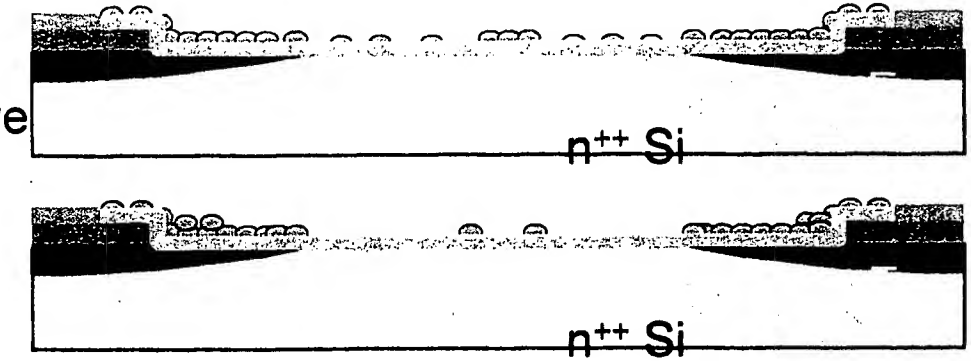
n++ Si

Local Pt areas destroyed

Thin TiOx e- chann ls

n++ Si

Effects of Annealing



Ctr-edge coalescence (high resistive ctr)

Edge coalescence (isolated center)

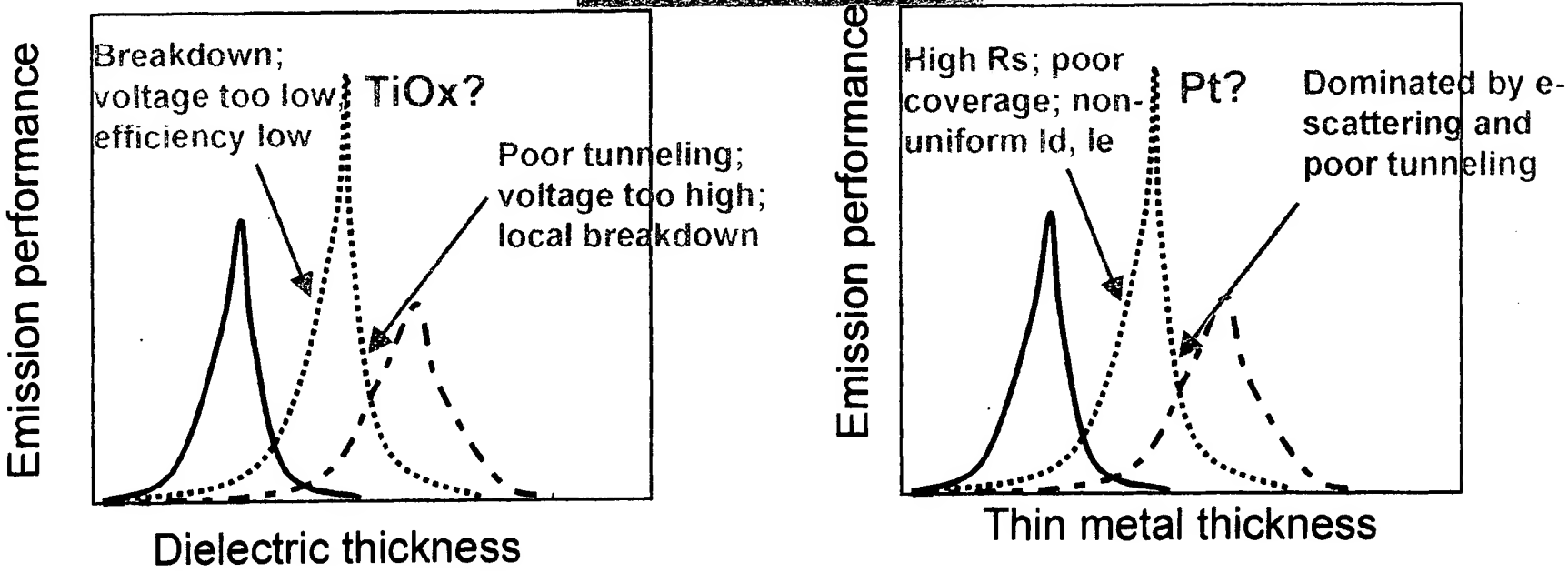
MIS Flat Emitters

MIS Material Optimization

- Dielectric? (TiOx, SiOx, M-matrix?) Thickness?
- Role of interfaces, defects?

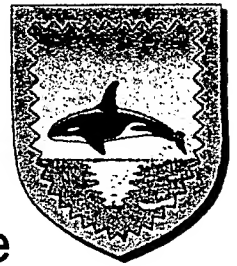
- Metal? (Pt, Pd, Au, Al, Ag…)
- Thickness?
- Role of interfaces? Annealing?

Where are we?



MIS Flat Emitters

Conclusions

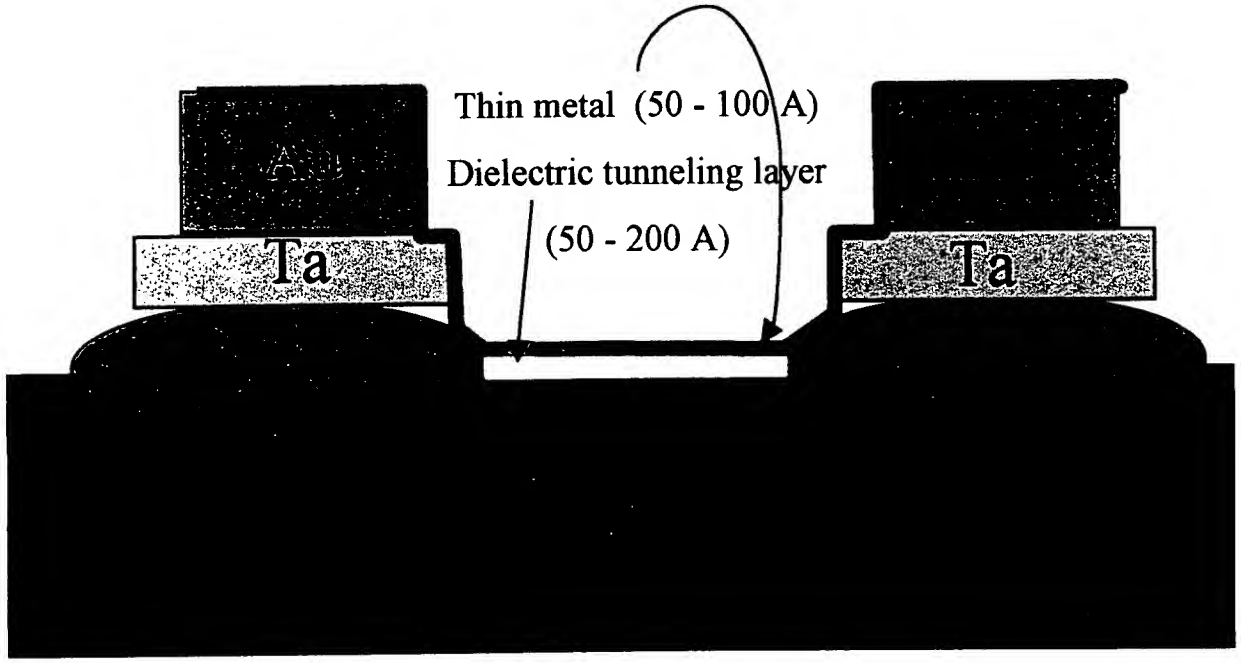


- We are at the beginning of understanding "MIS" device
  - Need to create emission sites and emit from same sites over emitter life. Key is density of sites.
  - Will probably always have spotted emission
  - Degradation, edge defects, flicker, lifetime can likely be improved but not in 1 month
- Expts leading up to mid-April DP Exit (MIS #3 TiOx)
  - Electroform optimization
  - Annealing conditions w/RTA (pre, post-Pt dep, temp, time)
  - Next expts in fab will not impact mid-April DP date
- Failure analysis + thought models
  - Want high density of emission sites as built-in characteristic of material. Porous Si or other 'fibrous' film may be best answer for high current requirements
  - However, no test results to indicate that P-Si is any better

Nano holes in thin metal layer- A key for the electron emission for flat emitter device

1. Nano holes provide electron emission sites which is a key for electron emission.
2. Nano holes may improve the emission reliability of emitters.
3. Nano holes reduce spiking and improves emission stability.
4. Nano holes can be produced in thin metal layer, such as Pt and Ta/AU by using appropriate annealing process.
5. Annealing ambient and temperature are the two critical process parameters to produce and control the nano holes. In this invention, we found that the temperature is in a range of 400C – 650 C, and nitrogen ambient is the key to generate the nano holes, while oxygen and Argon are not effective.

Flat emitter structure



Second generation process

1.define emission area by FOX

2. Ta/Au Deposition

3. Metal 1 photo patterning

4. Au wet etch

5 Ta dry etch

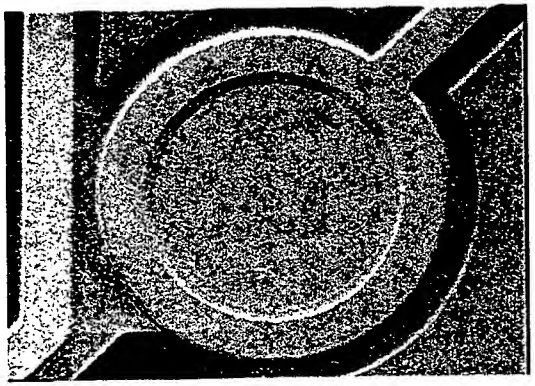
6. Tunneling layer dep./lift off

7. Top thin metal dep Pt or Ta/Au.

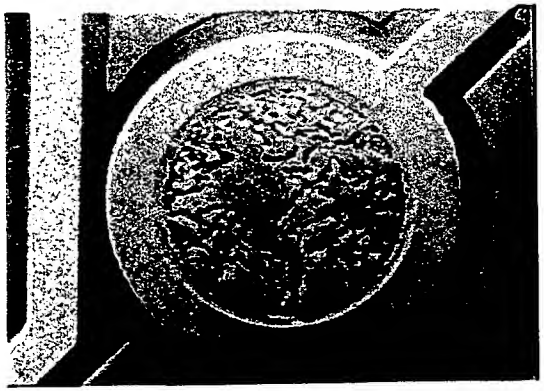
8. trench photo

9 .thin metal etch

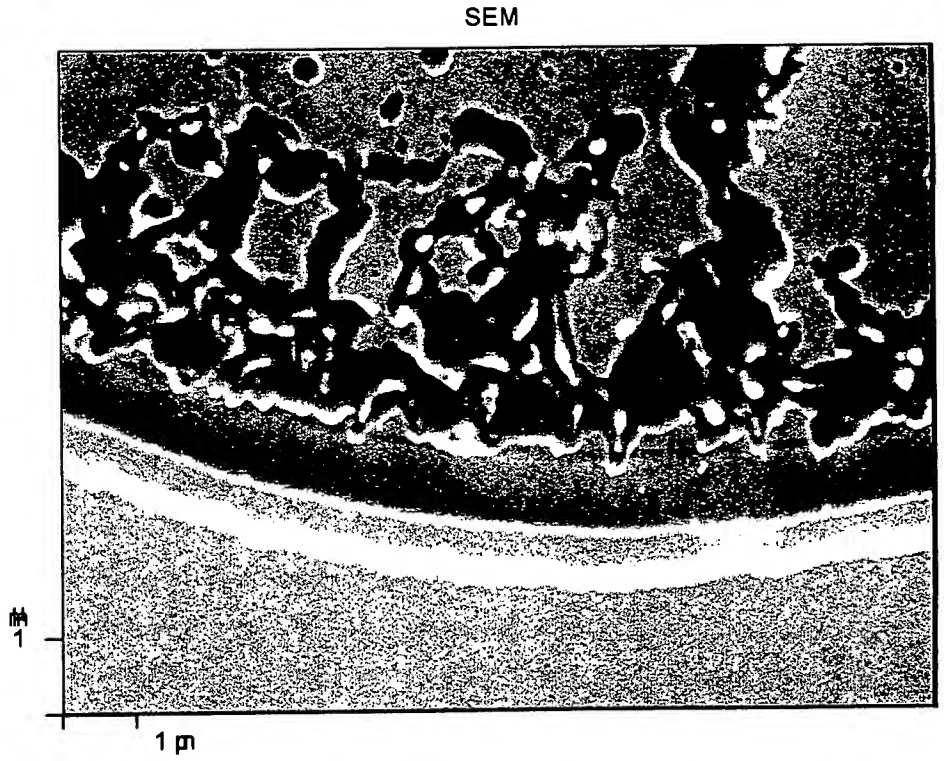
Electrical breakdown Damage on thin metal layer

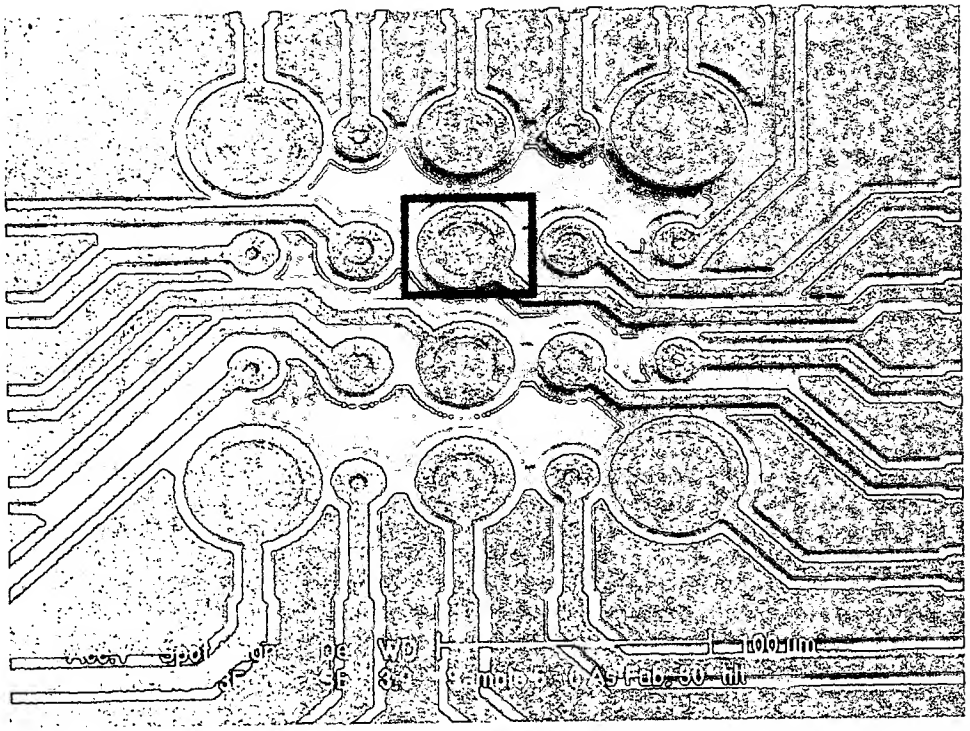


As deposit



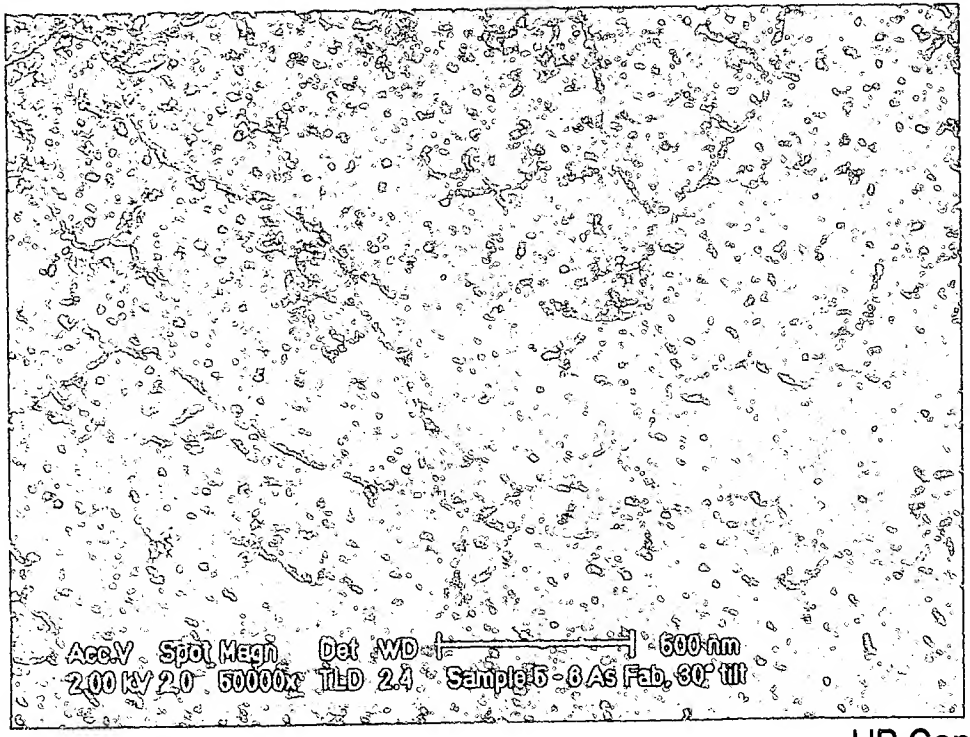
Early breakdown damage

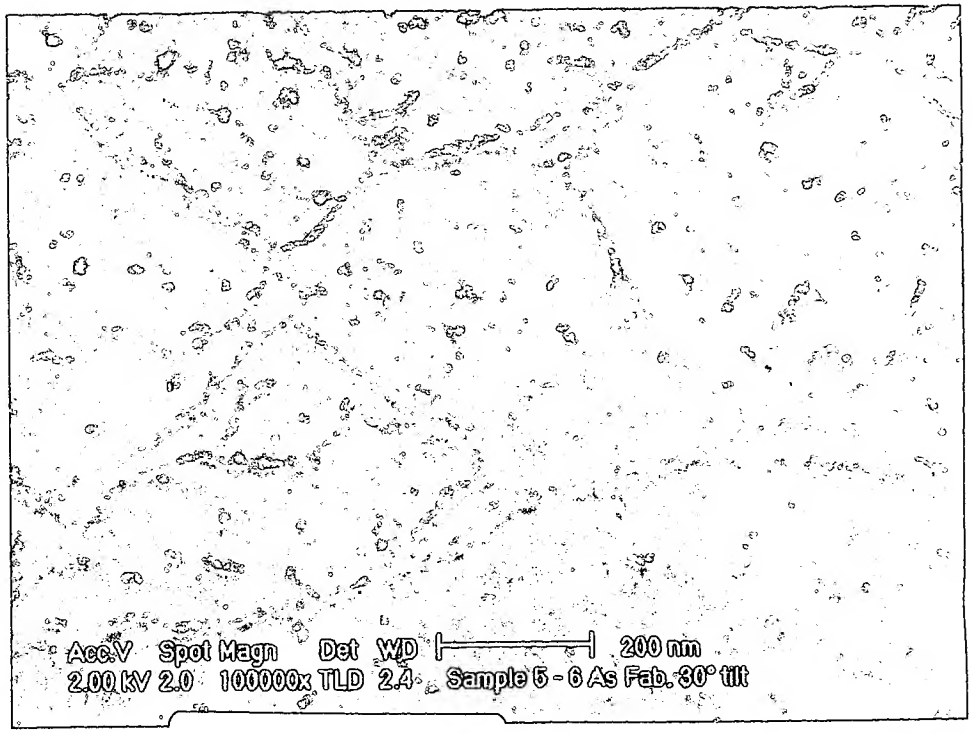


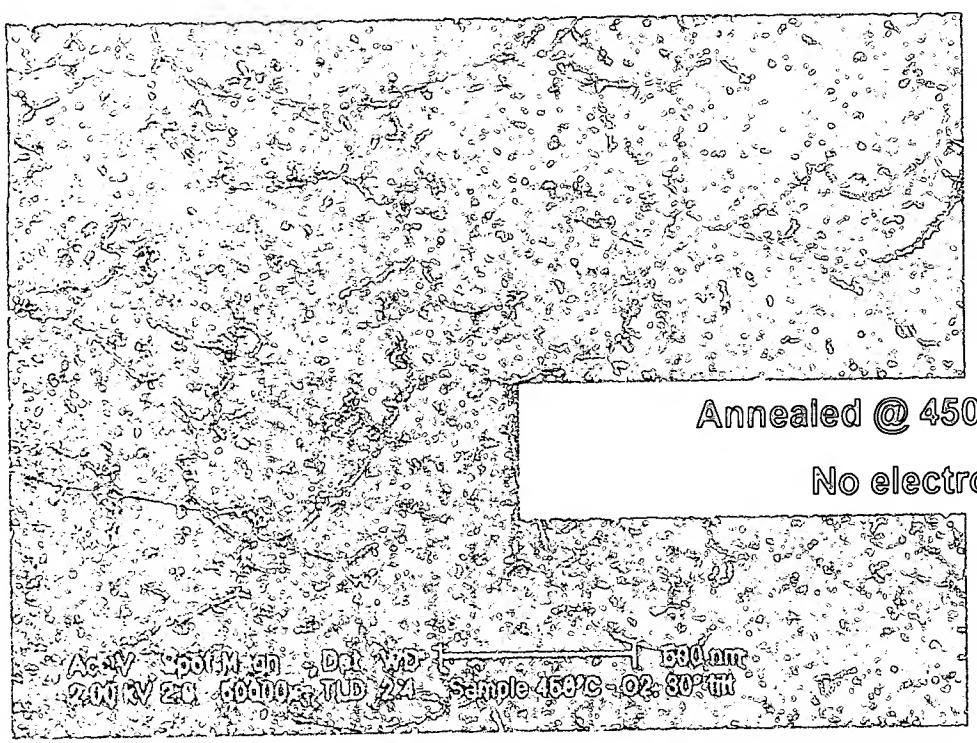


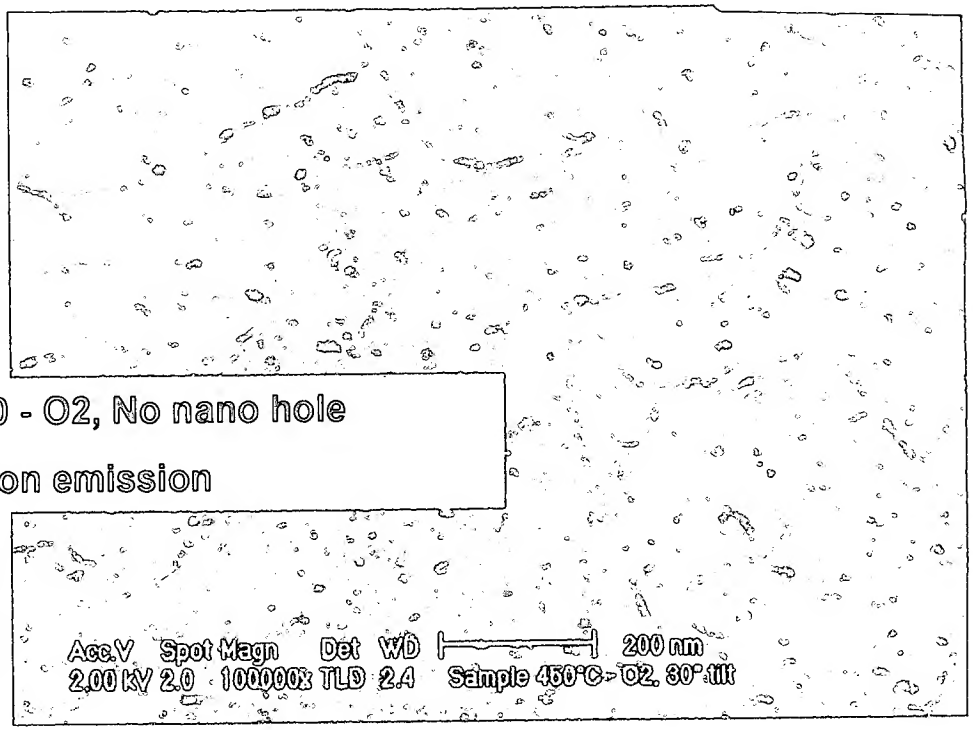
Nano hole development in thin metal

As deposited thin Pt film with thickness ~ 7nm
No nano holes structure in this film.
No electron emission.



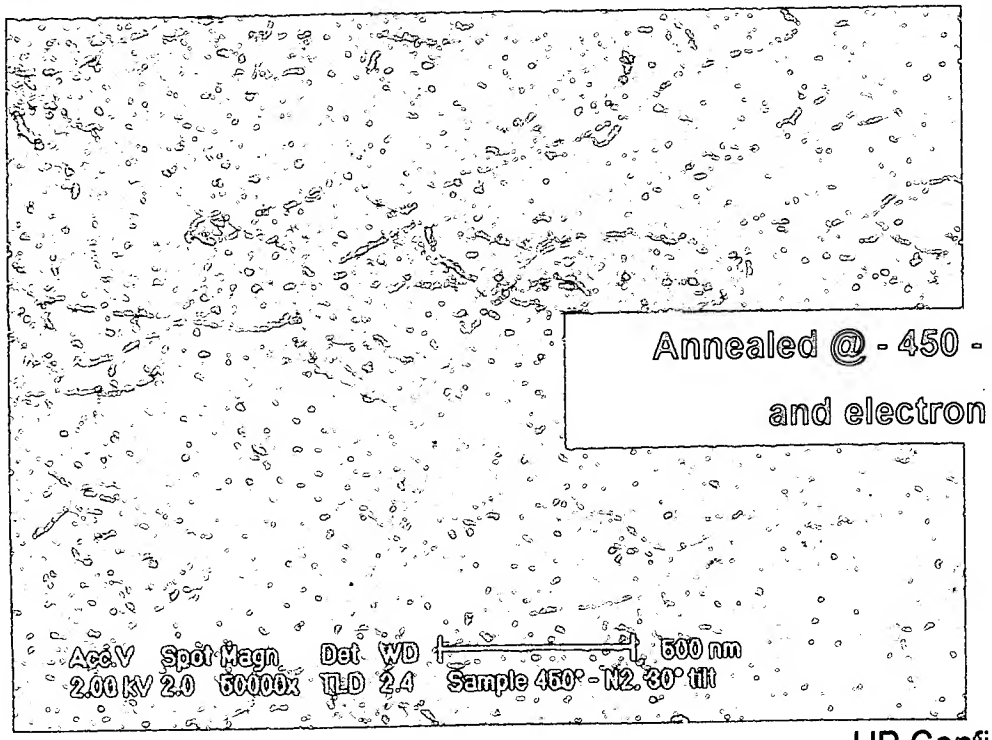


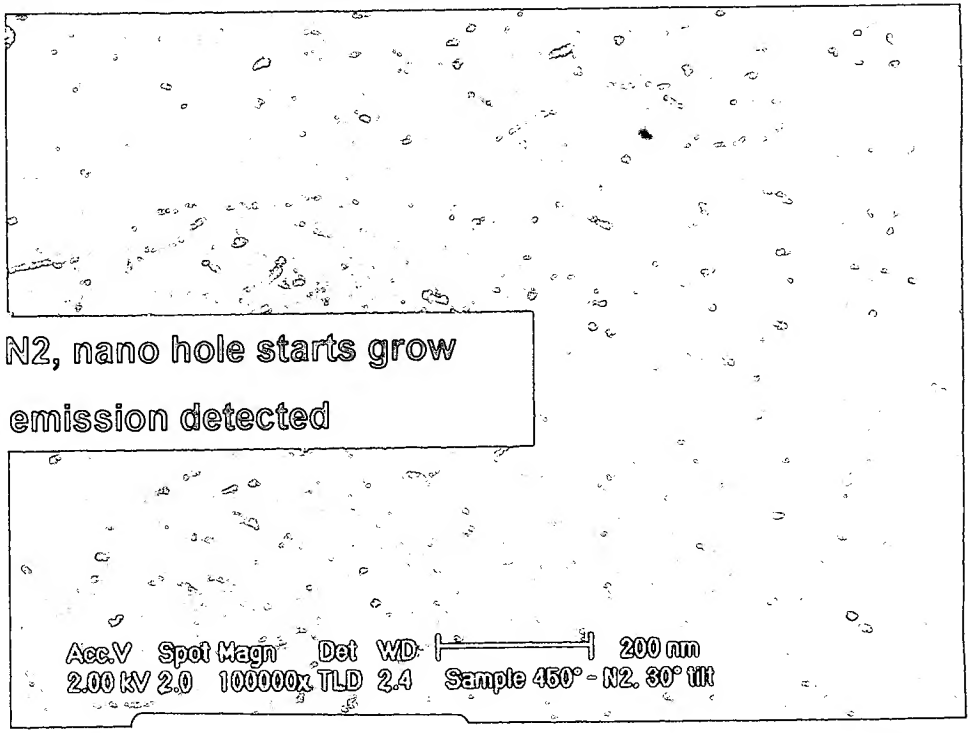




Annealed @ 450 - O2, No nano hole

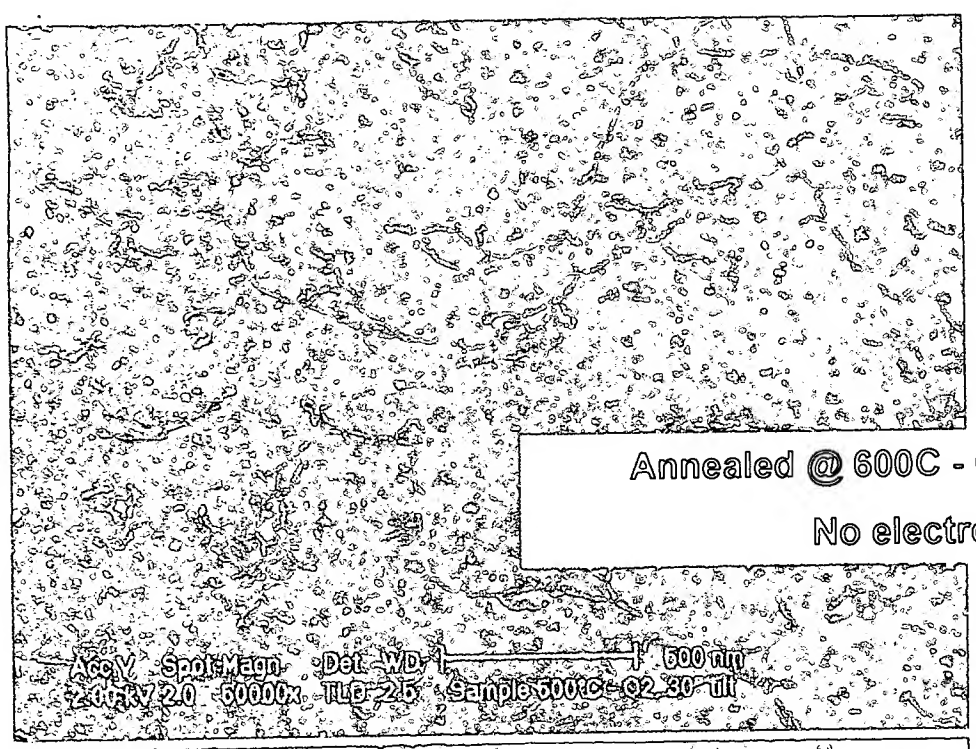
No electron emission

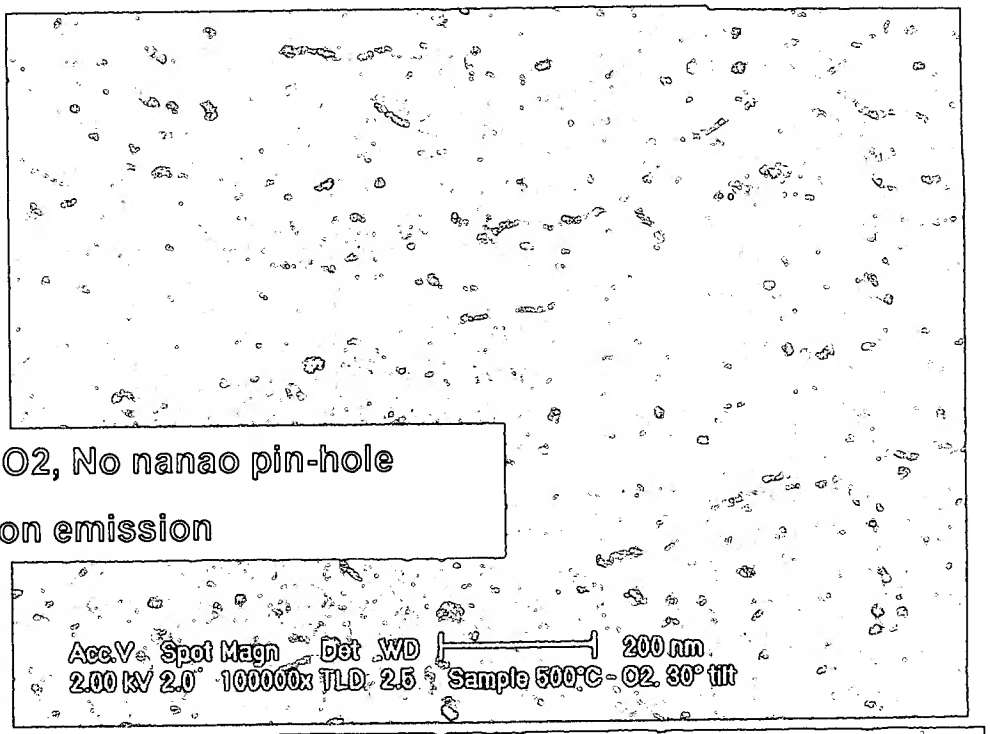




Annealed @ - 450 - N2, nano hole starts grow

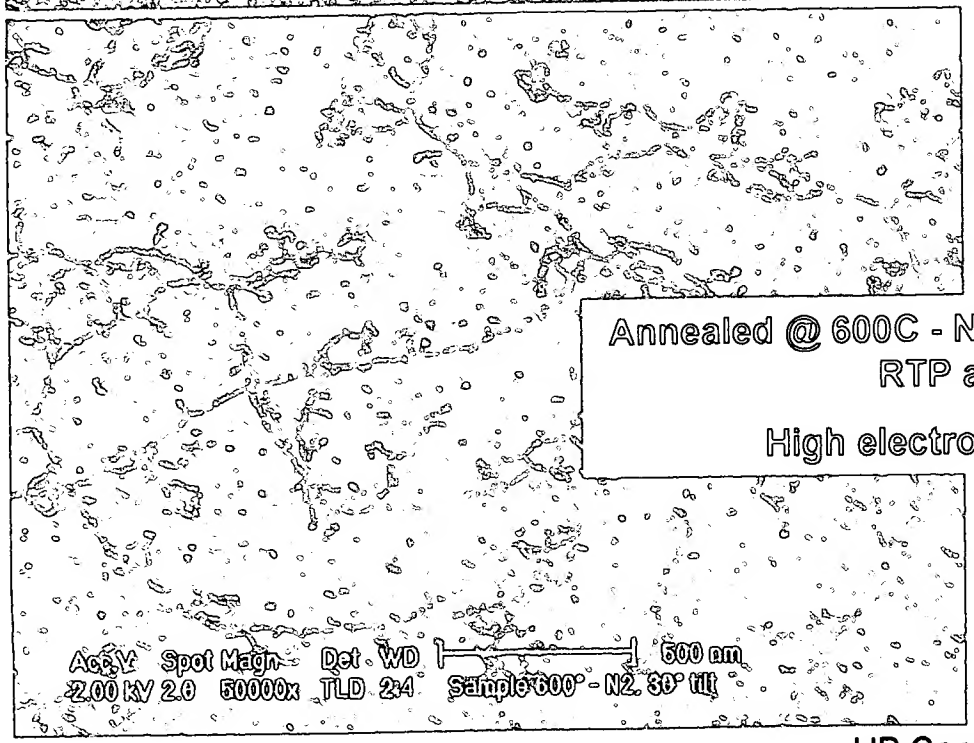
and electron emission detected

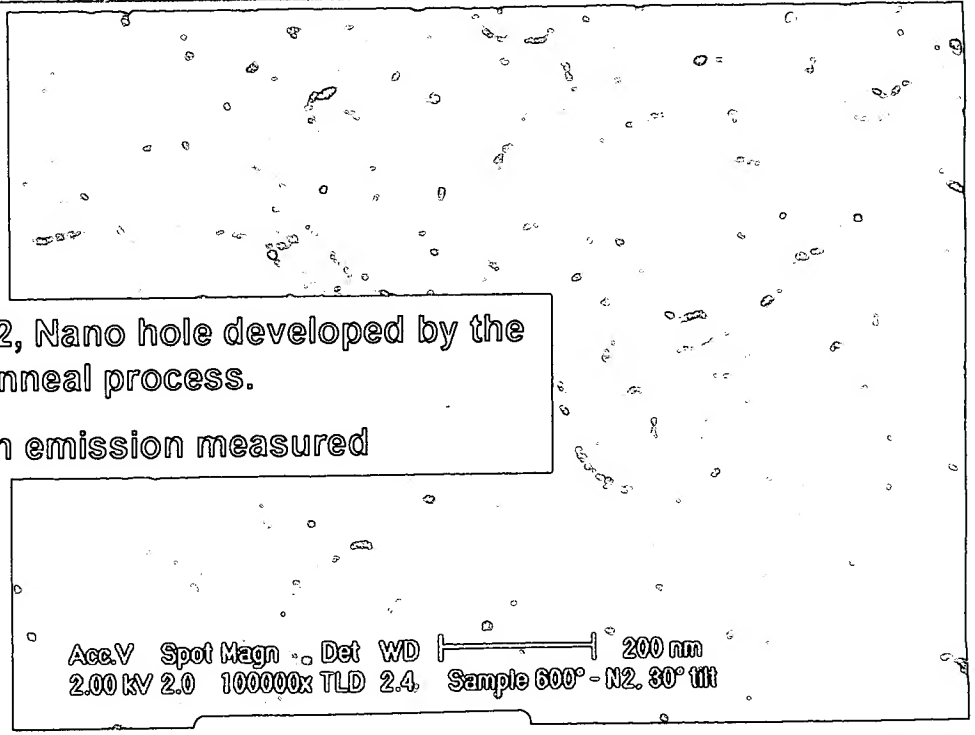




Annealed @ 600C - O2, No nanao pin-hole

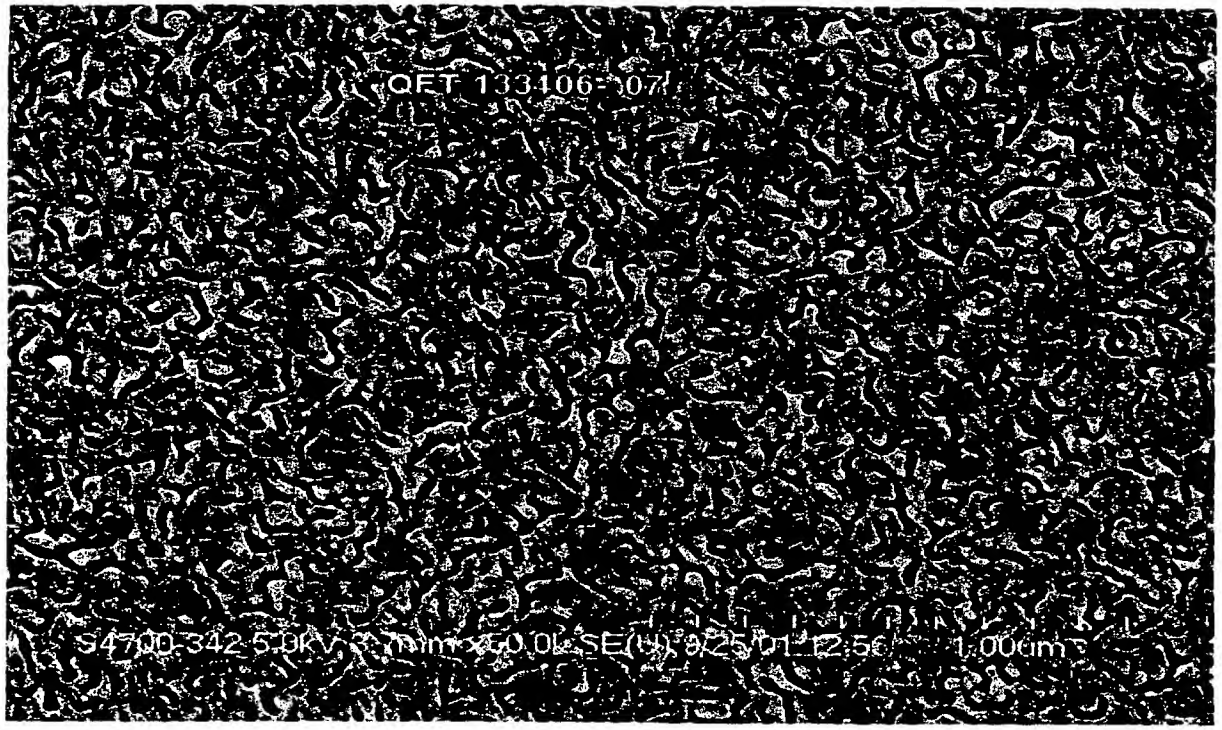
No electron emission





Annealed @ 600C - N2, Nano hole developed by the RTP anneal process.

High electron emission measured

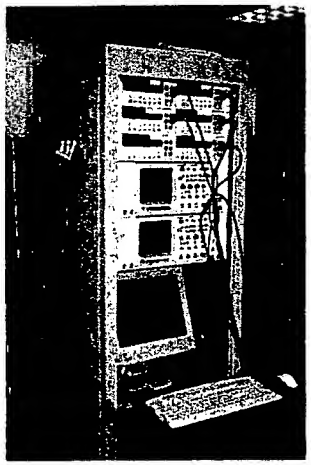


75A of Au on oxide

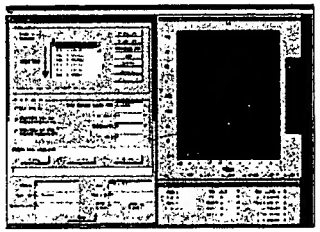
600°C N_2

Emitter Energy Testing

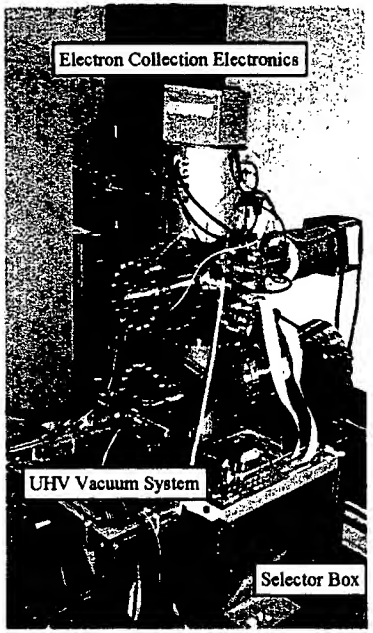
Chip Testers 2 and 4 are versatile, automated emission testers capable of accurately measuring emission and diode currents from Porous Silicon, MIS, and Spindt Tip emitters. The testers are a hybrid of commercially available instrumentation and custom instrumentation.

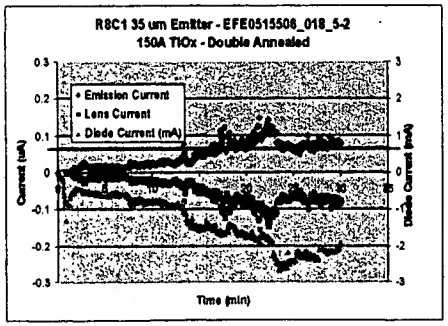


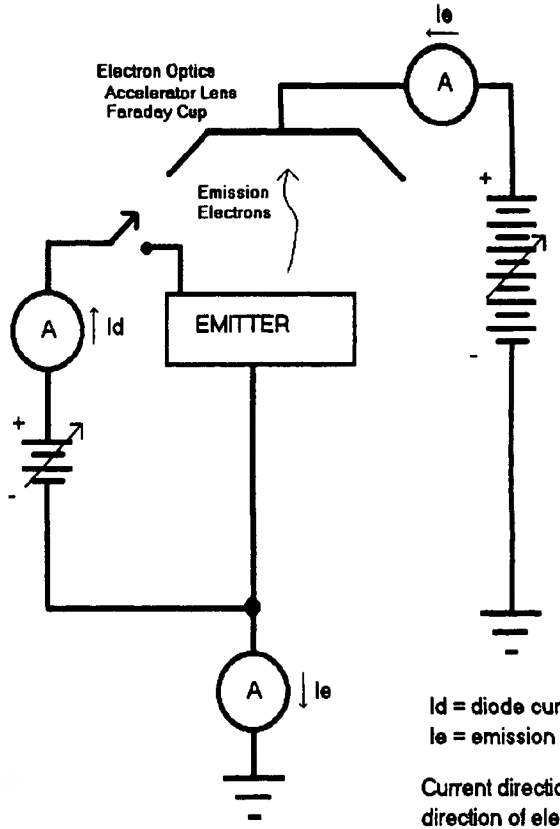
Data acquisition/control rack



Automated Software







Id = diode current
Ie = emission current

Current direction is opposite to direction of electron flow

Outputs (Voltages)	Range	Precision
Diode Voltage	0 to 100 Volts	1%
Focusing Voltage	-100 to 100 V	1%
Accelerator Lens	0 to 2000 Volts	1%
Faraday Cup Voltage	0 to 2000 Volts	1%
Inputs (Currents)		
Id (Diode Current)	-4 to 40 mA	.5 uA
Ie (Emission Current)	-6 to +6 uA	1 nA
I_{al} (Accelerator Lens Current)	-6 to +6 uA	.3 nA
I_{fc} (Faraday Cup Current)	-6 to +6 uA	.3 nA

TECHNOLOGY DEVELOPMENT OPERATIONS

hp invent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chen, Zhizhang, et al. Art Unit: 2822

Examiner: Lewis, Monica

Serial Number: 09/846,127

Filed: April 30, 2001

Title: TUNNELLING EMITTER

Date: August 1, 2002

DECLARATION UNDER RULE 132

I, Zhizang Chen, do hereby declare and say:

My home address is 4411 Snowbrush Dr., Corvallis, Oregon.

I have a BS and MS in Electronics from Nankai University, Tianjin, China, a MS in physics from Oregon State University and a Ph.D in Material Science Engineering from Virginia Tech.

I have worked in the semiconductor industry since 1985.

I have been employed by Hewlett-Packard Company for six years and have been at my current position as an R&D Engineer for two years.

Exhibit A, entitled "Direct Tunneling Emitter Process Development and Improvement" and dated 1/12/2001 is a status report presented to Hewlett-Packard management that describes the differences observed between annealed and unannealed metal cluster emitters. The data contained within is believed to be a true and accurate copy of data collected during experiments performed on test devices at Hewlett-Packard facilities.

Exhibit B, entitled "MIS Update – Planfest IV" and dated 3/20/2001 is a status report on further testing and failure analysis of the metal cluster emitters presented to Hewlett-Packard management. The data contained within the report is believed to be a true and accurate copy of data collected during experiments

performed at Hewlett-Packard facilities. The report lists the results of electrical testing on emission currents of the metal cluster emitters.

Exhibit C, entitled "Nano Holes in Thin Metal Layer – A Key for the Electron Emission for Flat Emitter Device" and undated is a Powerpoint slide presentation presented to Hewlett-Packard management. The data contained within the report is believed to be a true and accurate copy of data collected during experiments performed at Hewlett-Packard facilities. The report demonstrates the changes in the cathode layer due to the affects of annealing the metal cluster emitters.

Exhibit D, entitled "Emitter Energy Testing" and undated represents the test setup used to measure the diode and emission currents. This exhibit is presented to help the reader to better understand how the results listed in Exhibit B were obtained.

I further declare that all statements made herein of my own knowledge are true an that all statements made on information and belief are believed to be true; and that these statements were mad with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issuing thereon.

Signed:

Chen Zhizhang

Zhizhang Chen

Date: August 1, 2002